50272-101

REPORT DOCUMENTATION PAGE 1. AD-A207 865

3. Recipient's Accession No.

4. Title and Subtitle
Defense Communications Agency Circular
Defense Data Network
C/30E Physical Layer Interface Guide

5. Report Date
30 Jan 89 DOP

6.

7. Author(s)

8. Performing Organization Rept. No.
DCAC 350-180-( )

9. Performing Organization Name and Address
Defense Communications Agency
Defense Communications Engineering Center
Code R620
1860 Wiehle Avenue
Reston, VA 22090-5500

10. Project/Task/Work Unit No.

11. Contract(C) or Grant(G) No.
(C) N/A
(G)

12. Sponsoring Organization Name and Address
Defense Communications Agency
Defense Communications Engineering Center
1860 Wiehle Avenue
Reston, VA 22090-5500

13. Type of Report & Period Covered
DRAFT

14.

15. Supplementary Notes
Will be published as a final document at a later date.

16. Abstract (Limit: 200 words)
This draft circular prescribes the policy, assigns the responsibility, and identifies the requirements for connecting an X.25 host to a C/30E Packet Switched Node (PSN) on the Defense Data Network by means of a MIL-STD-188-114 (balanced), EIA-232-D, or V.35 interface. The circular also identifies the requirements for connecting one C/30E PSN to another. This circular will be published in final form at a later date.

17. Document Analysis a. Descriptors
Defense Data Network
Protocol (Computers)
Physical Layer

b. Identifiers/Open-Ended Terms
RS-449/422 or RS-449/423
RS-232-D
Mil-STD-188-114

c. COSATI Field/Group

18. Availability Statement	19. Security Class (This Report)	21. No. of Pages
Unlimited Release	Unclassified	96
	20. Security Class (This Page)	22. Price
	Unclassified	

(See ANSI-Z39.18) See Instructions on Reverse

OPTIONAL FORM 272 (4-77)
(Formerly NTIS-35)
Department of Commerce

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DCA CIRCULAR
350-180-( )

DEFENSE COMMUNICATIONS AGENCY

DEFENSE DATA NETWORK

C/30E PHYSICAL LAYER INTERFACE GUIDE

D R A F T

30 JAN 1989

GENERAL INFORMATION
C/30E Physical Level Interface Guide

1. Purpose. This Circular prescribes the policy, assigns the responsibility, and identifies the requirements for connecting an X.25 host to a C/30E PSN by means of a MIL-STD-188-114 (balanced), EIA-232-D, or V.35 interface. This Circular also identifies the requirements for connecting one C/30E PSN to another by means of a MIL-STD-188-114 (balanced), EIA-232-D, or V.35 interface, as well as for the BELL 303 interface. Keywords: DIGITAL COMPUTERS, ELECTRICAL TERMINALS - DEFENSE

2. Applicability. This Circular applies to Headquarters, DCA, and all subordinate and affiliate activities, and all military departments and Government agencies using or requesting DDN access.

3. References.

a. Military Standard 188-114; "Electrical Characteristics of Digital Interface Circuits," 24 March 1976.

b. EIA Standard 449; "General Purpose 37-Position and 9-Position Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange," November 1977.

c. EIA Standard 232-D; "Interface between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange," December 1985.

d. International Standard ISO 2593; "Connector Pin Allocations for Use with High-Speed Data Terminal Equipment," 1973-03-01 (First Edition).

e. Bell System Technical Reference; "Wideband Data Stations 303-Type," August 1966.

f. EIA Standard 530; "Interface between Data Terminal Equipment and Data Circuit-Terminating Eqipment Employing Serial Binary Data Interchange," March 1987.

4. Definitions. The following definitions are pertinent to this Circular.

a. C/30E. X.25-based communication processor made by BBN Communications Corporation. Used in Packet-Switching Network applications.

b. DCE. Data Circuit-Terminating Equipment.

c. DC-37P. 37-pin male connector.

d. DC-37S. 37-pin female connector.

e. DDN. Defense Data Network.

f. DPPC. Digital Patch Panel connected between the DCE and the encryption device.

g. DPPE. Digital Patch Panel connected between the DTE and the encryption device.

h. DTE. Data Terminal Equipment.

i. EIA. Electronic Industries Association.

j. EMI. Electromagnetic Interference.

k. FDBCLK. MSYNC-driven clock-sourcing MIL-STD-188-114 adapter (fantail) containing EIA-449 connectors. The FDBCLK fantail can be used to source clock.

l. FDB3. MSYNC-driven MIL-STD-188-114 fantail containing EIA-449 connectors. FDB3 cannot provide clock.

m. FD4. Fantail containing EIA-232-D connectors.

n. FPA. Fixed Plant Adapters: Complete assembly consisting of two KGABs, space for two KG-84As, and one FPA shelf that supports the assembly in the encryption cabinet.

o. KGAB. Interfaces a KG-84A with a communications line by providing for cable termination, filter isolation, and update counter support.

p. KG-84A. Provides standard link encryption to all interswitch trunks and host access lines on the MILNET. Not used for collocated equipment.

q. MII Board. Input/output motherboard used in C/30E PSNs to interface with communications lines leading to other DDN PSNs.

r. MMBC Board. Daughterboard emulating a MIL-STD-188-114 DCE, thus providing clock. Its DTE counterpart is the MMB board.

s. MMI Board. Daughterboard emulating a BELL 303 DTE.

t. MML Board. Daughterboard emulating a BELL 303 DCE.

u. MS Connection. KGAB Connectors.

v. MSYNC. Input/output motherboard that is used in C/30E PSNs to interface with synchronous host access lines.

w. PSN. Packet Switch Node used in the DDN to provide full service network access ports for hosts and trunks. PSN and C/30E are used interchangeably in this document.

x. Synchronous Devices. Require a clock signal to operate the communications interface.

y. TEMPEST. Limits compromising electromagnetic emanations from communications equipment.

z. Trunk. Communications link providing an interface between two nearby or remote PSNs, hence a PSN-to-PSN interface.

5. Policy.

a. The current DDN standard node supports only MIL-STD-188-114 balanced serial host interfaces. The EIA-232 and V.35 interfaces are not recommended for future installations, but they may be found where they are provided by an existing installation, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN standard. MIL-STD-188-114 is based on the RS-449 interface, a standard which manufacturers have stated will not be supported in the future. This will mean that future 188-114 procurements will be more expensive than necessary, necessitating adapter cables to match commonly available peripheral equipment as we move into the next decade. The industry is transitioning to EIA-530 as a standard for balanced serial interfaces. This interface employs the traditional 25 pin (RS-232 Connector) and is functionally compatible with the RS-449. The EIA-530 uses the electrical characteristics described in RS-422 or RS-423 standards. In response to OSD direction to reduce costs by acquiring commercial equipment using commercial standards, the EIA 530 standard shall be specified wherever possible in the future. Devices using an EIA-530 implementation may be connected by means of an adapted cable to the PSN's 37 pin EIA-449 connectors. A diagram is found in the references EIA-530 standard on page 34 (the first page of the appendix), "Interconnecting EIA-530 with EIA-449".

b. DDN policy is that the C/30E minimum host bit rate be 9.6 kb/s for MIL-STD-188-114, EIA-232-D, and V.35 interfaces. DDN also supports Extended Modem Looping (XMOD).

6. Responsibility. DCA, Code B611, will ensure that this Circular is updated to reflect current DDN standard node.

FOR THE DIRECTOR:

EDWARD R. CARWISE
Colonel, USAF
Chief of Staff

CONTENTS

ILLUSTRATIONS

Figure Page

CHAPTER 1. MIL-STD-188-114 NEIGHBOR OR NEARBY HOST INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the MIL-STD-188-114 balanced interface that connects the C/30E PSN with a collocated host. This interface is largely in conformance with the EIA-449/422 standard considered the general commercial equivalent to MIL-STD-188-114. Exceptions to the standard include the required signal states for Clear to Send and Receiver Ready as well as the open circuit voltage. For ease of reference, table 1-1 equates the EIA-449, EIA-232, and CCITT interface signal names. However, in the rest of chapters 1 and 2, only the EIA-449 signal name will be used.

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E 188-114 interface circuits are in accordance with MIL-STD-188-114, chapter 5, except with regard to subsection 5.1.1.3: Open Circuit Measurement. The C/30E open circuit driver voltage, measured in accordance with 5.1.1.3, is less than $\pm$9.0V for balanced drivers and $\pm$4.5V for unbalanced drivers.

b. Clocking. Two fantails, FDB3 and FDBCLK, provide the EIA-449 connectors that terminate cables from all I/O interfaces. The fantail connectors are configured as DTEs. When the FDB3 fantail is used, the host (DCE) must provide clock because the FDB3 fantail does not support clock-sourcing capability. When FDBCLK, a clock-sourcing enhanced fantail, is used, either the DTE or DCE can provide clock.

(1) FDB Fantail Clock Rates. FDBCLK and FDB3 interface hardware support any external clock between 1.2 kb/s and 112 kb/s. However, DDN policy is that the minimum PSN bit rate be 9.6 kb/s. When FDBCLK clock-sourcing capability is used, the FDBCLK on-board clock generator provides the frequencies described in table 1-2.

TABLE 1-2. FREQUENCIES PROVIDED BY THE FDBCLK FANTAIL

Clock Frequency	Accuracy*
112kHz, 56kHz, 19.2kHz,9.6kHz, 4.8kHz, 2.4kHz	$\pm$0.05% (500 ppm**)
64kHz, 50kHz	$\pm$0.005% (50 ppm)

* Accuracy over a temperature range of 10 to 30 degrees C.
** PPM = Parts Per Million

TABLE 1-1. SIGNAL NAME EQUIVALENCY TABLE

EIA-449 ID	EIA-449 Name	EIA-232-D ID	EIA-232-D Name	CCITT ID
SG	Signal Ground	AB	Signal Ground	102
SC	Send Common	--		102a
RC	Receive Common	--		102b
SD	Send Data	BA	Transmitted Data	103
RD	Receive Data	BB	Received Data	104
RS	Request To Send	CA	Request To Send	105
CS	Clear To Send	CB	Clear To Send	106
DM	Data Mode	CC	Data Set Ready (DCE Ready)	107
TR	Terminal Ready	CD	Data Terminal Ready (DTE Ready)	108/2
RR	Receiver Ready	CF	Received Line Signal Detector	109
IS	Terminal In Service	--		---
SQ	Signal Quality	CG	Signal Quality Detector	110
SR	Signaling Rate Selector	CH	Data Signal Rate Selector (DTE Source)	111
SI	Signaling Rate Indicator	CI	Data Signal Rate Selector (DCE Source)	112
NS	New Signal	--		---
TT	Terminal Timing	DA	Transmitter Signal Element Timing (DTE Source)	113
ST	Send Timing	DB	Transmitter Signal Element Timing (DCE Source)	114
RT	Receive Timing	DD	Receiver Signal Element Timing	115
SS	Select Standby	--		116
SB	Standby Indicator	--		117
IC	Incoming Call	CE	Ring Indicator	125
SF	Select Frequency	--		126
LL	Local Loopback	LL	Local Loopback	141
RL	Remote Loopback	RL	Remote Loopback	140
TM	Test Mode	TM	Test Mode	142
AT	Alternate Timing*	--		142

* Alternate Timing is provided on spare pins 3 and 21 when the FDBCLK clock-sourcing fantail is providing clock.

(2) Signaling Sense. Signaling sense for balanced and unbalanced circuits is in accordance with EIA-422-A with the exception that the differential voltage applied to the interconnecting cable is in the range of 2 volts to 9 volts for the C/30E. As defined in RS-422-A, ON (0, Space, or +) is generated when A terminal is positive with respect to the B terminal, and OFF (1, MARK, or -) is generated when A terminal is negative with respect to the B terminal.

c. Bit Rate and Cable Length. Interconnecting cable length and its relation to data signaling rates is in accordance with EIA Standard 449, section 6.10, and EIA Standard 422-A, section 4.3 and the appendix.

(1) Maximum Cable Length. The maximum length of the cable is 1000 feet.

(2) Slew Rate Limiting. Signal rise time is set to 1 microsecond (100 kb/s value).

d. Interchange Circuits. The EIA-449 interface for the C/30E is provided by the MSYNC motherboard in conjunction with the appropriate daughterboards to fulfill the MIL-STD-188-114 I/O option.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in table 1-3.

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: either the software reacts to the circuit signal when it changes, or the software can assert a circuit when necessary (such as LL which can be used by operations personnel for testing connections). Unsupported circuits either are not read by the software or a value is written to the circuit by the software and that value does not change during operation. Table 1-3 provides a list of circuits and their use.

(3) Interchange Circuit Definitions. For additional information about these interchange circuits, see EIA Standard 449. The following descriptions assume use of full period/full duplex circuits, with flow control handled at higher levels.

(a) Signal Ground. See EIA Standard EIA-449.

(b) Send Common. See EIA Standard EIA-449.

(c) Receive Common. See EIA Standard EIA-449.

(d) Terminal in Service. IS is tied ON by the hardware.

(e) Incoming Call. IC is reported to the Monitoring Center; however, its value has no software effect.

(f) Terminal Ready. TR is asserted ON by PSN software when the link is initialized.

(g) Data Mode. DM must be asserted ON by the DCE and is monitored by the PSN software.

(h) Send Data. See EIA Standard EIA-449.

(i) Receive Data. See EIA Standard EIA-449.

(j) Terminal Timing. See EIA Standard EIA-449.

(k) Send Timing. See EIA Standard EIA-449.

(l) Receive Timing. See EIA Standard EIA-449.

(m) Request to Send. RS is asserted ON by PSN software when the link is initialized.

(n) Clear to Send. CS must be asserted ON by the DCE and is monitored by PSN software. If the signal state on this line changes to OFF, the software macrocode will stop data transmission.

(o) Receiver Ready . RR must be asserted ON by the DCE and is monitored by PSN software. If the signal state on this line changes to OFF, the software macrocode will stop receiving data.

(p) Signal Quality. SQ is reported to the Monitoring Center; however, its value has no software effect.

(q) New Signal. NS is tied OFF by the hardware.

(r) Select Frequency. SF/SR is electrically active and asserted OFF by the PSN software when the link is initialized.

(s) Signaling Rate Selector. SF/SR is electrically active and asserted OFF by the PSN software when the link is initialized.

(t) Signaling Rate Indicator. SI is reported to the Monitoring Center; however, its value has no software effect.

(u) Local Loopback. LL is electrically active, but asserted OFF by PSN software when the link is initialized. LL can be controlled by the Monitoring Center.

(v) Remote Loopback. RL is electrically active, but asserted OFF by PSN software when the link is initialized. RL is available for Monitoring Center control.

(w) Test Mode. TM is reported to the Monitoring Center; however, its value has no software effect.

TABLE 1-3. DDN STANDARD NODE INTERCHANGE CIRCUIT USE

449 ID	EIA-449 Name	Source	Electrical Circuit	Required State of Control/Status Sigals
SG	Signal Ground	DTE/DCE	Ground	N/A
SC	Send Common	DTE	Ground	N/A
RC	Receive Common	DCE	Ground	N/A
SD	Send Data	DTE	Active	N/A
RD	Receive Data	DCE	Active	N/A
RS	Request to Send	DTE	Active	ON
CS	Clear to Send	DCE	Active	ON
DM	Data Mode	DCE	Active	ON
TR	Terminal Ready	DTE	Active	ON
RR	Receiver Ready	DCE	Active	ON
SQ	Signal Quality	DCE	Active	Don't Care
SF/SR	Select Frequency/ Signaling Rate Sel.	DTE	Active	OFF
SI	Signaling Rate indicator	DCE	Active	Don't Care
TT	Terminal Timing	DTE	Active	N/A
ST	Send Timing	DCE	Active	N/A
RT	Receive Timing	DCE	Active	N/A
SS	Select Standby	DTE	Static	OFF
SB	Standby Indicator	DCE	Not Connected	Don't Care
IC	Incoming Call	DCE	Active	Don't Care
LL	Local Loopback	DTE	Active	OFF
RL	Remote Loopback	DTE	Active	OFF
TM	Test Mode	DCE	Active	Don't Care
NS	New Signal	DTE	Static	OFF
IS	Terminal in Service	DTE	Static	ON
AT	Alternative Timing	DTE	Active	N/A

NOTE: N/A = Not Applicable

(x) Select Standby. SS is tied OFF by hardware.

(y) Stanby Indicator. SB is not connected.

3. Mechanical Characteristics. All EIA-449/422 connectors offered for the C/30E meet the following specifications.

a. Interface Connectors. All C/30E EIA-449 connectors are DC-37P type (male) connectors.

(1) Intermating dimensions are in accordance with EIA-449, section 3.3.1.

(2) The means for C/30E DTE connectors to latch and unlatch from the latching blocks on the DCE connector are within the dimensions specified in EIA-449, section 3.3.2. DDN uses the English 4-40 thread latching block.

b. Connector Contact Assignments. All C/30E EIA-449/422 contact assignments are in accordance with EIA-449, section 3.4. Table 1-4 provides the DDN standard node connector pinout. The signals are used as specified in section 2.d.3.

4. Interconnecting Cables.

a. Interconnecting cables are in accordance with MIL-STD-188-114. They must be low capacitance, multiple twisted pair that meet the following specifications resulting in a transmission line with a nominal characteristic impedance on the order of 100 ohms to frequencies greater than 100 kHz, and a dc series loop resistance not exceeding 240 ohms. The overall braid shield must have at least 85% coverage.

(1) Conductor Size. Interconnecting cables should be in accordance with MIL-STD-188-114, Appendix C, with regard to conductor size (subsection 30.3.1). Interconnecting cables or wires should be composed of wires of a 24 AWG or larger conductor for solid or stranded copper wires, or for non-copper conductors a sufficient size to yield a dc wire resistance not to exceed 30 ohms/1000 feet per conductor.

(2) Mutual Pair Capacitance. In accordance with MIL-STD-188-114, the capacitance between one wire in the pair to the other wire in the pair should not exceed 20 picofarads/foot, and the value should be reasonably uniform over the length of the wire or cable.

(3) Stray Capacitance. In accordance with MIL-STD-188-114, the capacitance between one wire in the cable to all others in the cable sheath, with all others connected to ground, should not exceed 40 picofarads/foot, and should be reasonably uniform for a given conductor over the length of the wire or cable.

TABLE 1-4. DDN STANDARD NODE EIA-449 (DTE) CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
1	FG		Frame Ground
2	SI	111	Signaling Rate Indicator
20	RC	102b	Receive Common
3	AT	---	Alternate Timing +
21	AT	---	Alternate Timing -
4	SD	103	Send Data +
22	SD	103	Send Data -
5	ST	114	Send Timing +
23	ST	114	Send Timing -
6	RD	104	Receive Data +
24	RD	104	Receive Data -
7	RS	105	Request to Send +
25	RS	105	Request to Send -
8	RT	115	Receive Timing +
26	RT	115	Receive Timing -
9	CS	106	Clear to Send +
27	CS	106	Clear to Send -
10	LL	141	Local Loopback
28	IS	---	Terminal in Service
11	DM	107	Data Mode +
29	DM	107	Data Mode -
12	TR	108.2	Terminal Ready +
30	TR	108.2	Terminal Ready -
13	RR	109	Receiver Ready +
31	RR	109	Receiver Ready -
14	RL	140	Remote Loopback
32	SS	116	Select Standby
15	IC	125	Incoming Call
33	SQ	110	Signal Quality
16	SF/SR	126	Select Frequency/Signaling Rate Selector
34	NS	---	New Signal
17	TT	113	Terminal Timing +
35	TT	113	Terminal Timing -
18	TM	142	Test Mode
36	SB	117	Standby Indicator
19	SG	102	Signal Ground
37	SC	102a	Send Common

(4) Pair-to-Pair Balanced Crosstalk. In accordance with MIL-STD-188-114, Appendix C, with regard to pair-to-pair balanced crosstalk (subsection 30.3.4), the crosstalk from on pair of wires to any other pair in the same cable sheath should have a minimum value of 40 dB of attenuation measured at 150 kHz.

(b) Figure 1-1 is a cabling diagram of a C/30E PSN connected to a nearby EIA-449 host, and figure 1-2 is an example of a cable (BBNCC P/N# 2409313G01) that could be used to interconnect them.

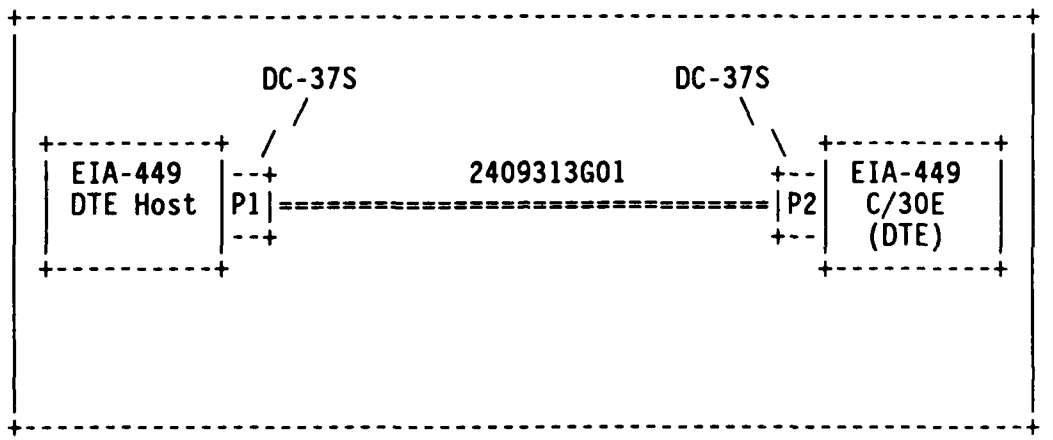


FIGURE 1-1. C/30E PSN AND NEARBY EIA-449 HOST CABLING DIAGRAM (C/30E SOURCES CLOCK)

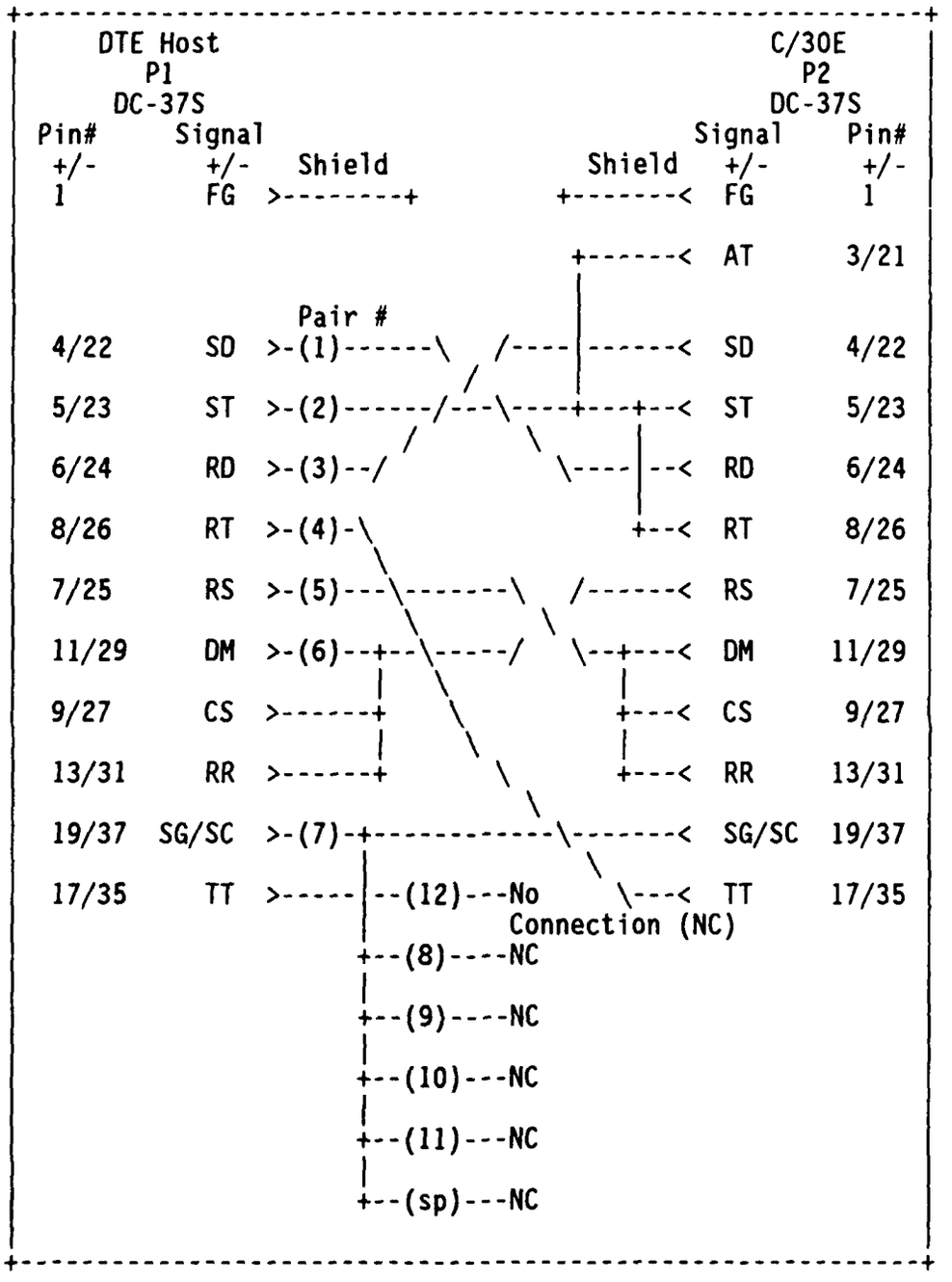


FIGURE 1-2. CABLE EXAMPLE: C/30E PSN TO EIA-449 NEARBY HOST (C/30E SOURCES CLOCK)

CHAPTER 2. MIL-STD-188-114 REMOTE HOST INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the MIL-STD-188-114 balanced remote host interface. This chapter documents the interface between the remote modem and the host (demarcation point A in figure 2-1) with no intervening cryptographic devices (KG-84As). Eventually KG-84As will be required for all host access circuits; therefore, figure 2-2 provides an example of the cabling that connects the remote modem to the remote Fixed Plant Adapter (FPA) and then to the host (demarcation point B in figure 2-2).

2. Electrical Characteristics.

a. Voltage Levels. The modems used will conform to EIA-449. The electrical interface of the KG-84A is in accordance with MIL-STD-188-114, chapter 5, except with regard to subsection 5.1.1.3: Open Circuit Measurement. The open circuit driver voltage, measured in accordance with 5.1.1.3, is less than ±10.0V for balanced drivers and ±5.0V for unbalanced drivers.

b. Clocking.

(1) Modem Clocking. The modem supplies timing on the Send Timing and Receive Timing circuits. Terminal Timing is not supported for remote host interfaces. While the DDN hardware will support between 1.2 kb/s and 64 kb/s, DDN policy is that the minimum host access rate be 9.6 kb/s.

(2) Signaling Sense. Signaling sense for balanced and unbalanced circuits is in accordance with EIA-422-A with the exception of the differential voltage, which when applied to the interconnecting cable, is in the C/30E range of 2 volts to 9 volts. As defined in RS-232-A, ON (0, Space, or +) is generated when the A terminal is positive with respect to the B terminal, and OFF (1, MARK, or -) is generated when the A terminal is negative with respect to the B terminal.

c. Bit Rate and Cable Length.

(1) EIA-449 Compliance. Interconnecting cable length and its relation to data signaling rates is in accordance with EIA Standard 449, section 6.10, and EIA Standard 422-A, section 4.3 and the appendix.

(2) Maximum Cable Length. The maximum cable length between the remote modem and the host including the intervening FPA is 1000 feet; however, cable lengths less than 200 feet are preferred.

d. Interchange Circuits.

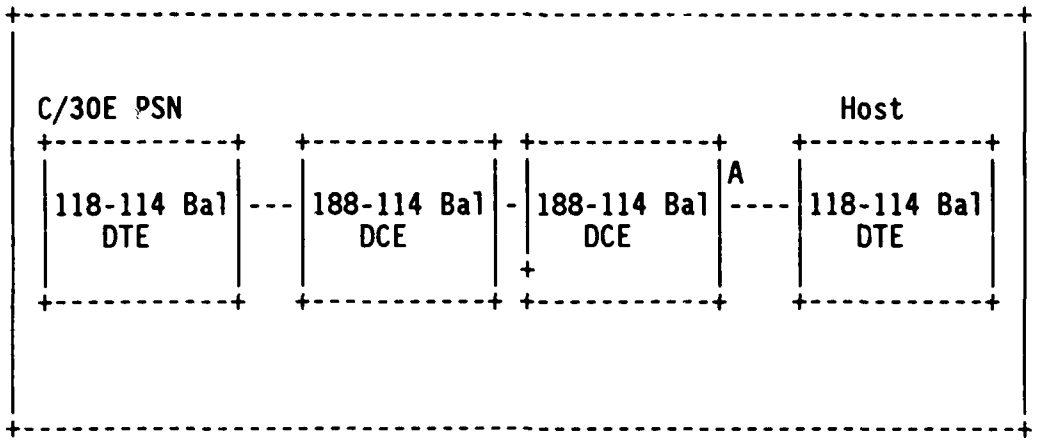


FIGURE 2-1. DEMERCATION POINT "A" BETWEEN THE C/30 AND REMOTE HOST

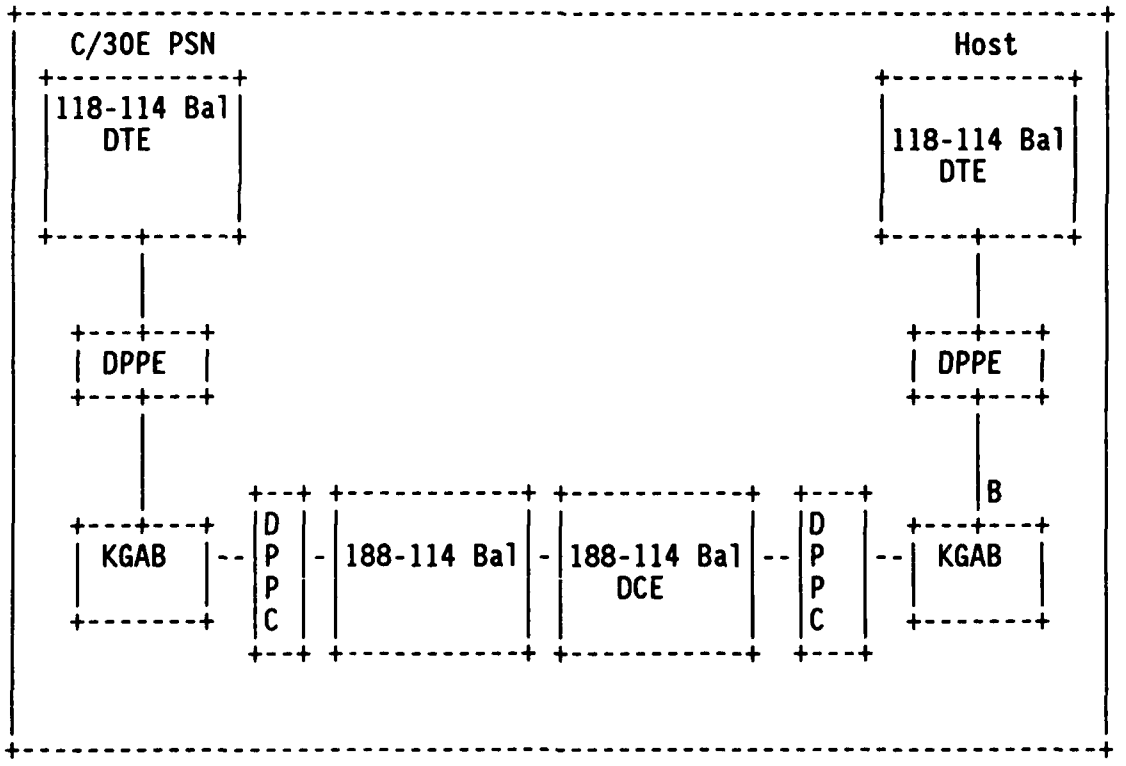


FIGURE 2-2. DEMARCATION POINT "B" BETWEEN THE KGAB AND HOST

(1) C/30E Local Modem Interface.

(a) Signal flow between the C/30E and the local modem is shown in figure 2-3. This interface and associated hardware are provided by DDN. The signal flow is the same when a KG-84A is used. This interface uses EIA-449 pin assignments.

(b) As shown in figure 2-3, the supported signals are Send Data (SD), Send Timing (ST), Receive Data (RD), Receive Timing (RT), and Terminal Ready (TR). Clear to Send (CS), Data Mode (DM), and Receiver Ready (RR) are tied ON by the cable connected to the fantail. Remote Loopback (RL) and Local Loopback (LL) are to be used for those functions and they are connected at the DCE interface. Terminal Timing (TT) is not supported from the PSN.

(c) Two special DDN-specific loopback signals, C[illegible]DL, are provided as shown in figure 2-3. The Signaling Rate Selector (SR) signal is used by the PSN to loop the local KG-84A and is designated as "C" loop or CL (standing for COMSEC Loopback) in figure 2-3 after it leaves the C/30E fantail. SR is not connected to the DCE interface. The Request To Send (RS) signal is reserved for future use within the FPA KG-84A and is designated as "D" loop or DL. RS is not connected at the DCE interface. The Terminal Ready (TR) signal from the PSN provides both the Terminal Ready and Request to Send (RS) to the DCE.

(2) Host-Remote Modem Interface. The cable functional signal flow between the remote modem and the DTE host is also shown in figure 2-3. The signal flow is the same as that described in 1.d.1, above. The KGAB uses MS connectors with the pinout shown in figure 2-3 and tables 2-2 and 2-3. Figure 2-3 shows DDN standard cables. Figure 2-2 is provided as an example of one way to connect to a remote host. If DDN standard cables are not used, only the signals shown as mandatory in table 2-2 are required. The optional signals are used by the PSN end of the circuit.

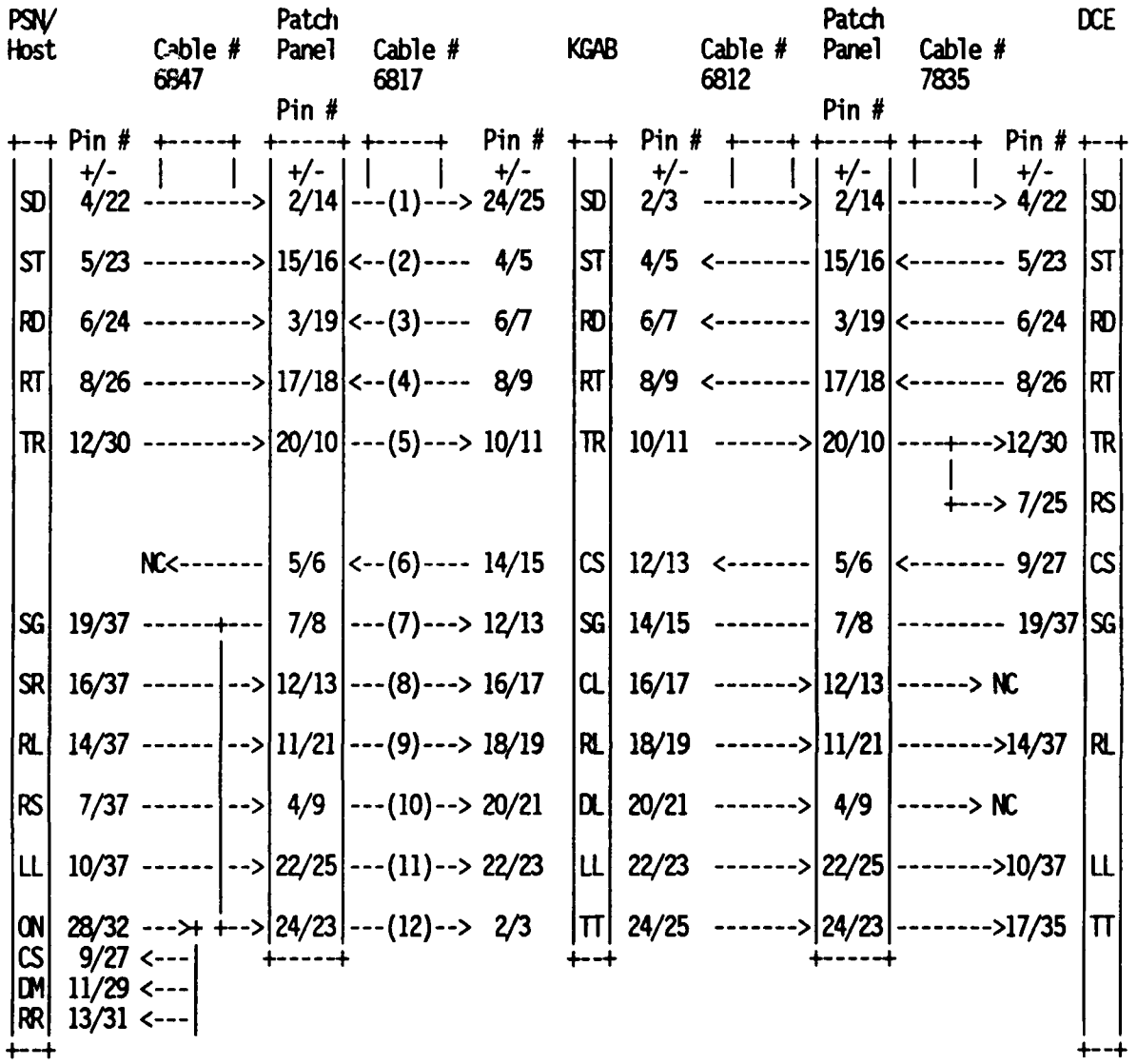
3. Mechanical Characteristics. All EIA-449/422 connectors offered for the C/30E meet the specifications provided in this section.

a. Interface Connectors. DDN MIL-STD-188-114 DCE connectors are DC-37S type (female) connectors. The DDN FPA uses an MS connector on the KGAB counter assemblies.

b. Connector Contact Assignments.

(1) C/30E Connectors. All DDN EIA-449/422 contact assignments are in accordance with EIA-449, section 3.4. In chapter 1, table 1-5 provides the standard DTE pinouts and section 2.d.3 provides circuit descriptions.

(2) KGAB Connectors. KGAB connectors to the remote host and the remote modem are shown in tables 2-2 and 2-3, respectively.



Notes: 1. Pin numbers are the same on both sides of Patch Panel.
2. Encircled numbers are the cable pair numbers.

FIGURE 2-3. FUNCTIONAL SIGNAL FLOW BETWEEN A NEARBY MODEM AND C/30E OR A KGAB AND A REMOTE HOST

TABLE 2-1. REMOTE-MODEM DTE INTERFACE CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
4	SD +	103	Send Data
22	SD -	103	Send Data
5	ST +	114	Send Timing
23	ST -	114	Send Timing
6	RD +	104	Receive Data
24	RD -	104	Receive Data
7	RS +	105	Request to Send
25	RS -	105	Request to Send
8	RT +	115	Receive Timing
26	RT -	115	Receive Timing
9	CS +	106	Clear to Send
27	CS -	106	Clear to Send
12	TR +	108.2	Terminal Ready
30	TR -	108.2	Terminal Ready
17	TT +	113	Terminal Timing
35	TT -	113	Terminal Timing
19	SG	102	Signal Ground
37	SC	102a	Send Common
Optional			
2	SI	112	Signaling Rate Indicator
10	LL	141	Local Loopback
11	DM +	107	Data Mode
13	RR	109	Receiver Ready
14	RL	140	Remote Loopback
15	IC	125	Incoming Call
16	SF/SR	126/111	Select Frequency/Signaling Rate
Selector			
18	TM	142	Test Mode
20	RC	102b	Receive Common
28	IS	---	Terminal In Service
29	DM -	107	Data Mode
31	RR -	109	Receiver Ready
32	SS	116	Select Standby
33	SQ	110	Signal Quality
34	NS	---	New Signal
36	SB	117	Standby Indicator

TABLE 2-2. KGAB - REMOTE HOST CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
24	SD +	103	Send Data
25	SD -	103	Send Data
4	ST +	114	Send Timing
5	ST -	114	Send Timing
6	RD +	104	Receive Data
7	RD -	104	Receive Data
8	RT +	115	Receive Timing
9	RT -	115	Receive Timing
10	TR +	108.2	Terminal Ready
11	TR -	108.2	Terminal Ready
12	SG	102	Signal Ground
13	SC	102a	Send Common
19	SS	116	Select Standby
Optional			
14	CS +	106	Clear to Send
15	CS -	106	Clear to Send
22	LL	141	Local Loopback
20	DL +	105	"D" Loop (Reserved)
21	DL -	105	"D" Loop (Reserved)
18	RL	140	Remote Loopback
2	TT +	113	Terminal Timing
3	TT -	113	Terminal Timing
16	CL +	126	"C" Loop (KG-84A Loop)
17	CL -	126	"C" Loop (KG-84A Loop)

TABLE 2-3 KGAB - REMOTE MODEM CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
2	SD +	103	Send Data
3	SD -	103	Send Data
4	ST +	114	Send Timing
5	ST -	114	Send Timing
6	RD +	104	Receive Data
7	RD -	104	Receive Data
8	RT +	115	Receive Timing
9	RT -	115	Receive Timing
10	TR +	108.2	Terminal Ready
11	TR -	108.2	Terminal Ready
14	SG	102	Signal Ground
15	SG	102	Signal Ground
24	TT +	113	Terminal Timing
25	TT -	113	Terminal Timing
Optional			
12	CS +	106	Clear To Send
13	CS -	106	Clear To Send
16	CL	---	"C" Loop (KG-84A Loop)
17	CL -	---	"C" Loop (KG-84A Loop)
18	RL +	140	Remote Loopback
19	RL -	140	Remote Loopback
20	DL +	---	"D" Loop (Reserved)
21	DL -	---	"D" Loop (Reserved)
22	LL +	141	Local Loopback
23	LL -	141	Local Loopback

4. Interconnecting Cables. Figures 2-4 and 2-5 provide a cabling diagram of a configuration with a C/30E, modems, and FPAs. Table 2-4 describes the cables used for interconnecting these devices. See chapter 1, section 4, for specifications on interconnecting cables.

TABLE 2-4. REMOTE INTERFACE CABLES

Connection	BBNCC P/N#	Description
PSN/Host to DPPE	2406847G01	12-pr, PSN/MSYNC 188-114 Bal Host to DB25P
DPPE to KGAB	2406817G01	12-pr, DB25S to FPA-J1
KGAB to DPPC	2406812G01	12-pr, FPA-J2 to DB25P
DPPC to DCE	2407835G01	12-pr, DB25S to 188-114 DCE

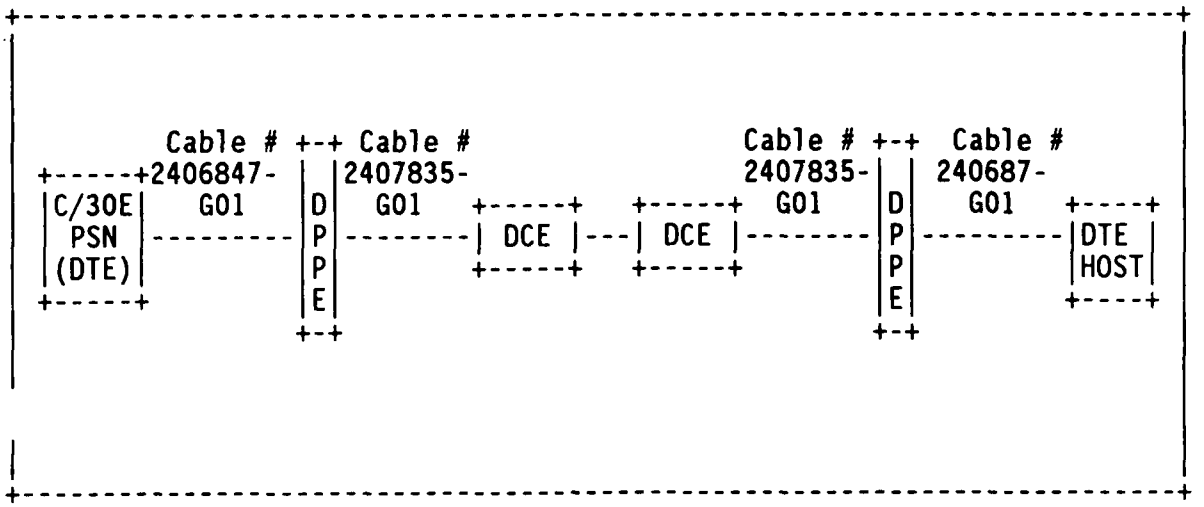


FIGURE 2-4. C/30E AND REMOTE HOST CABLING DIAGRAM

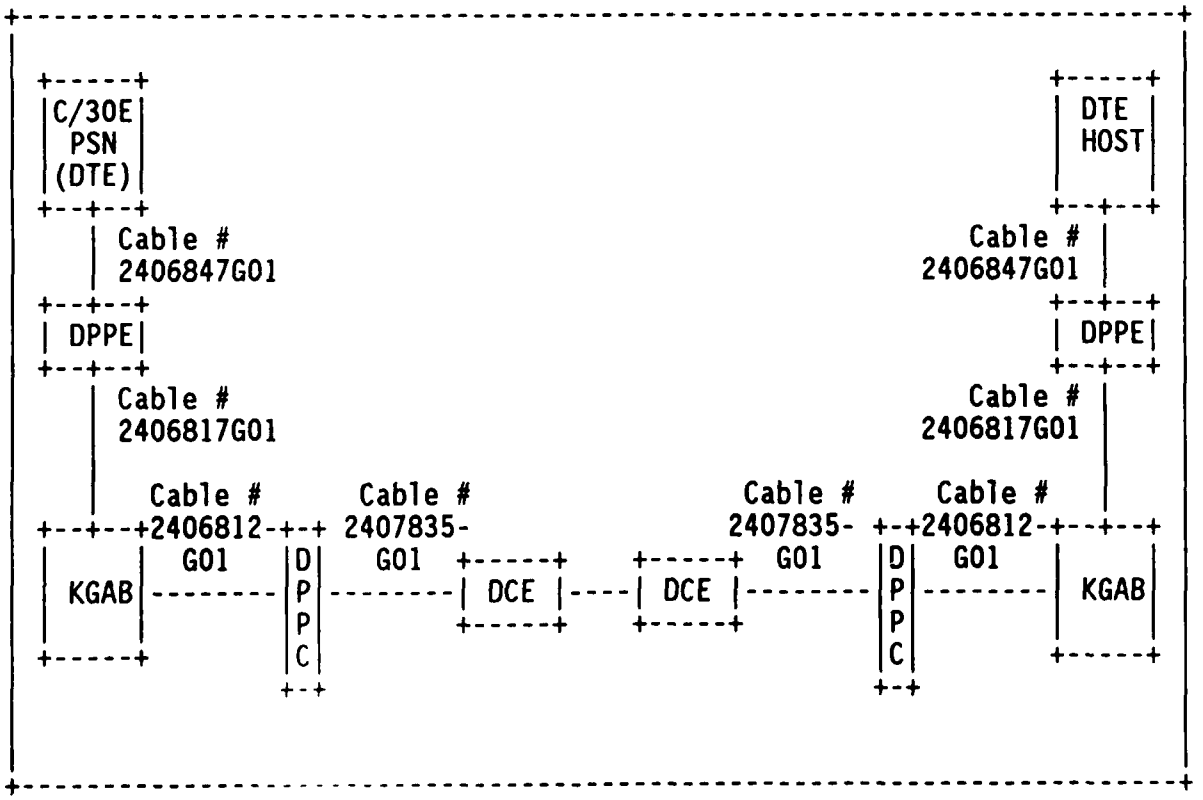


FIGURE 2-5. C/30E AND REMOTE HOST CABLING DIAGRAM
(WITH CRYPTOGRAPHIC DEVICES)

CHAPTER 3. EIA-232-D HOST INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the obsolete DDN EIA-232-D connection at the neighbor or nearby host. For ease of reference, table 3-1 equates the EIA-232-D, EIA-449, and CCITT interface signal names. However, in the rest of this chapter, only the EIA-232-D signal name will be used. DDN uses the EIA-232-D interface only where an existing non-DDN standard PSN provides such an interface, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN standard (MIL-STD-188-114 balanced serial host interfaces).

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E EIA-232-D interface circuits are in accordance with EIA Standard 232-D, section 2.1. For normal operation, the open circuit driver voltage shall be no more than $\pm$15 V.

b. Clocking.

(1) Supported Clock Rates. The FD4 fantail contains the connectors that terminate cables from all I/O interfaces. The FD4 fantail contains four EIA-232-D connectors configured as DTEs. This interface has clock-sourcing capability allowing either the DTE or DCE to provide the clock. The hardware can support external clock rates between 1.2 kb/s and 112 kb/s. However, DDN policy is 9.6 kb/s for the minimum PSN bit rate, and 19.2 kb/s for the maximum rate.

(2) Signaling Sense. Signaling sense is in accordance with EIA Standard 232-D, subsection 2.1.3. The signal is considered marking (OFF) when the voltage on the interchange circuit is more negative than -3 V with respect to signal ground, and spacing (ON) when the voltage is more positive than +3 V with respect to signal ground.

c. Bit Rate and Cable Length. Interconnecting cable length is in accordance with EIA-232-D, section 3.1. The recommended maximum cable length between an EIA-232-D DCE and DTE is 200 feet when overall shielded, low capacitance, twisted pair cable is used.

d. Interchange Circuits.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in table 3-2.

TABLE 3-1. SIGNAL NAME EQUIVALENCY TABLE

EIA-232-D ID	EIA-232-D Name	EIA-449 ID	EIA-449 Name	CCI ID
AB	Signal Ground	SG	Signal Ground	102
CE	Ring Indicator	IC	Incoming Call	125
CD	DTE Ready	TR	Terminal Ready	108
CC	DCE Ready	DM	Data Mode	107
BA	Transmitted Data	SD	Send Data	103
BB	Received Data	RD	Receive Data	104
DA	Transmitter Signal Element Timing (DTE Source)	TT	Terminal Timing	113
DB	Transmitter Signal Element Timing (DCE Source)	ST	Send Timing	114
DD	Receiver Signal Element Timing (DCE Source)	RT	Receive Timing	115
CA	Request To Send	RS	Request To Send	105
CB	Clear To Send	CS	Clear To Send	106
CF	Received Line Signal Detector	RR	Receiver Ready	109
CG	Signal Quality Detector	SQ	Signal Quality	110
CH	Data Signal Rate Selector (DTE Source)	SR	Signaling Rate Selector	111
CI	Data Signal Rate Selector (DCE Source)	SI	Signaling Rate Indicator	112
LL	Local Loopback	LL	Local Loopback	141
RL	Remote Loopback	RL	Remote Loopback	140
TM	Test Mode	TM	Test Mode	142

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: either the software reacts to the circuit signal when it changes, or the software can assert a circuit when necessary (such as LL which can be used by operations personnel for testing connections). Unsupported circuits either are not read by the software or a value is written to the circuit by the software, and that value does not change during operation. Table 3-2 provides a list of circuits and their use.

(3) Interchange Circuit Definitions.

(a) Signal Ground. See EIA Standard 232-D.

(b) Ring Indicator. RI is reported to the Monitoring Center; however, its value has no software effect.

(c) DCE Ready. This circuit must be asserted ON by the DCE, and it is monitored by the PSN software.

(d) DTE Ready. This circuit is asserted ON by PSN software when the link is initialized.

(e) Transmitted Data. See EIA Standard 232-D.

(f) Received Data. See EIA Standard 232-D.

(g) Transmitter Signal Element Timing (DTE Source). See EIA Standard 232-D. Also see subsection 2.b of this guide. This circuit provides the clock for Transmitted Data when the PSN sources timing. The frequency of this circuit should be equal to that of DTE-Sourced Receiver Signal Element Timing.

(h) Transmitter Signal Element Timing (DCE Source). See EIA Standard 232-D. This circuit provides the clock for Transmitted Data when the DCE sources timing.

(i) Receiver Signal Element Timing (DTE Source). This circuit provides the clock for Received Data when the PSN sources timing. The frequency of this circuit should be equal to that of DTE-Sourced Transmitter Signal Element Timing.

(j) Receiver Signal Element Timing (DCE Source). See EIA Standard 232-D. This circuit provides clock for Received Data when the DCE sources timing.

(k) Request to Send. This circuit is asserted ON by PSN software when the link is initialized.

(l) Clear to Send. CS must be asserted ON by the DCE and is monitored by PSN software to determine line status. If the signal state on this line changes to OFF, the software macrocode will stop data transmission.

(m) Received Line Signal Detector. This circuit must be asserted ON by the DCE as it is monitored to determine line status. If the signal state on this line changes to OFF, the software macrocode will stop receiving data.

(n) Signal Quality Detector. This circuit is reported to the Monitoring Center; however, its value has no software effect.

(o) Data Signal Rate Selector (DTE Source). This circuit is asserted OFF by the PSN software when the link is initialized.

(p) Data Signal Rate Selector (DCE Source). This circuit is electrically active; however, its value has no software effect.

(q) Local Loopback. LL is electrically active, but asserted OFF by PSN software when the link is initialized. LL can be controlled by the Monitoring Center.

(r) Remote Loopback. RL is electrically active, but asserted OFF by PSN software when the link is initialized. This circuit is available for Monitoring Center control.

(s) Test Mode. TM is reported to the Monitoring Center; however, its value has no software effect.

3. Mechanical Characteristics. All EIA-232-D connectors on the C/30E meet the specifications provided in this section.

a. Interface Connectors. All C/30E fantail MSYNC EIA-232-D connectors are DB-25P type (male) connectors. Intermating dimensions are in accordance with EIA-232-D, section 3.2.1.

b. Connector Contact Assignments. DDN standard node EIA-232-D connector contact assignments are in accordance with EIA-232-D, section 3.3.1. Table 3-3 provides DDN EIA-232-D connector pin assignments. Signal use is specified in section 2.d.3.

TABLE 3-2. EIA-232-D INTERCHANGE CIRCUIT USE

232 ID	EIA-232-D Name	Source	Electrical State	Required State of Control/Status Signals	Comm
AB	Signal Ground	DTE/DCE	Ground	N/A*	
BA	Transmitted Data	DTE	Active	N/A	
BB	Received Data	DCE	Active	N/A	
CA	Request to Send	DTE	Active	ON	
CB	Clear to Send	DCE	Active	ON	
CD	DTE Ready	DTE	Active	ON	
CF	Received Line Signal Detector	DCE	Active	ON	
CG	Signal Quality Detector	DCE	Active	Don't Care	
CH	Data Signal Rate Selector	DTE	Active	OFF	
CI	Data Signal Rate Selector	DCE	Active	Don't Care	
DA	Transmitter Signal Element Timing	DTE	Active	N/A	
DB	Transmitter Signal Element Timing	DCE	Active	N/A	
DC**	Receive Signal Element Timing	DTE	Active	N/A	
DD	Receive Signal Element Timing	DCE	Active	N/A	
CE	Ring Indicator	DCE	Active	Don't Care	
LL	Local Loopback	DTE	Active	OFF	
RL	Remote Loopback	DTE	Active	OFF	
TM	Test Mode	DCE	Active	Don't Care	

* N/A = Not Applicable
** The circuit name "DC" is from an earlier version of EIA-232.

TABLE 3-3. EIA-232-D CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
1	--	--	Shield
2	BA	103	Transmitted Data
3	BB	104	Received Data
4	CA	105	Request To Send
5	CB	106	Clear To Send
6	CC	107	DCE Ready
7	AB	102	Signal Ground (Common Return)
8	CF	109	Received Line Signal Detector
11	--	126	Select Transmit Frequency
15	DB	114	Transmitted Signal Element Timing (DCE Source)
17	DD	115	Receiver Signal Element Timing (DCE Source)
18	LL	141	Local Loopback
19	DC*	---	Receiver Signal Element Timing (DTE Source)
20	CD	108/2	DTE Ready
21	CG	110	Signal Quality Detector
22	CE	125	Ring Indicator
23	CH/CI	111/112	Data Rate Selector
24	DA	113	Transmit Signal Element Timing (DTE Source)
25	--	142	Test Indicator

* The circuit name "DC" is from an earlier version of EIA-232.

4. Interconnecting Cables.

a. For interconnecting cable specifications, see chapter 1, section 4, of this guide.

b. Figure 3-1 is a cabling diagram of a C/30E PSN connected to a nearby EIA-232 host, and figure 3-2 is an example of an interconnecting cable (BBNCC P/N# 2409318G01).

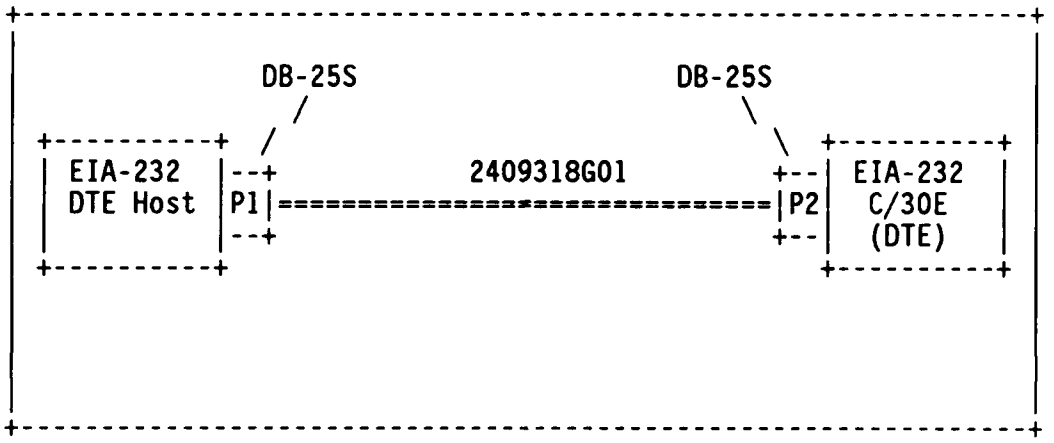


FIGURE 3-1. C/30 PSN AND NEARBY EIA-232-D HOST CABLING DIAGRAM

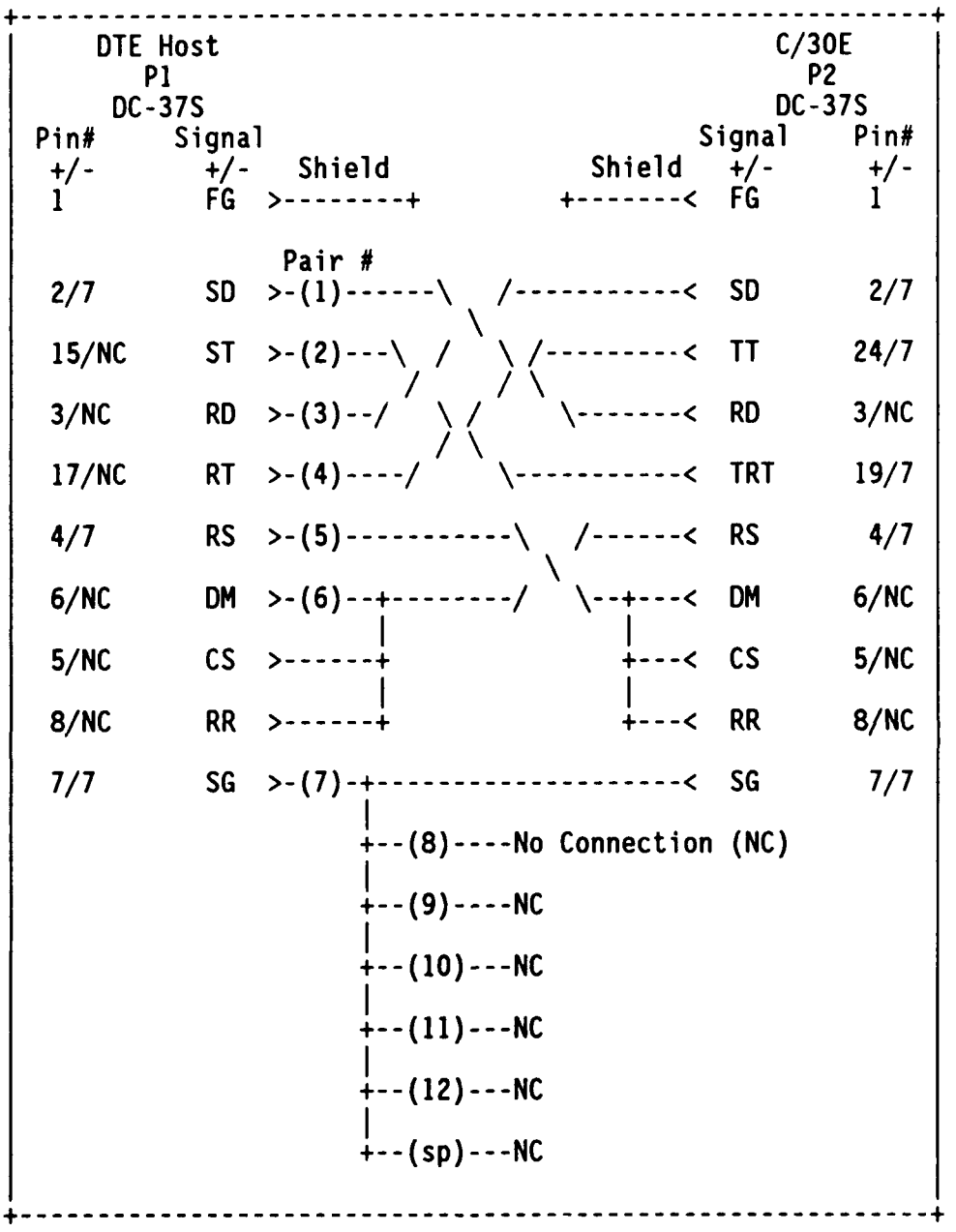


FIGURE 3-2. CABLE EXAMPLE: C/30E PSN TO NEARBY EIA-232-D HOST

CHAPTER 4. V.35 HOST INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the obsolete DDN V.35 connection at the neighbor or nearby host. All control signals have electrical characteristics of EIA-232-D, and EIA-232-D signal names are used in the rest of this chapter. The data and timing signals conform to Recommendation V.35. Like the EIA-232-D interface, the V.35 interface is used only where an existing non-DDN-standard PSN provides such an interface, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN-standard (MIL-STD-188-114 balanced serial host interfaces).

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E V.35 interface circuits are in accordance with CCITT Recommendation V.35.

b. Clocking. The FD4 fantail contains the connectors that terminate the cables from all I/O interfaces. The FD4 fantail contains four V.35 connectors configured as DTEs. This interface has clock-sourcing capability allowing either the DCE or C/30E to provide

the clock. The hardware can support external clock rates between 300 b/s and 100 kb/s. Three internal clocks are provided at the following rates: 76.8 kb/s, 57.6 kb/s, 9.6 kb/s.

(1) Signaling Sense. Signaling sense is in accordance with CCITT Recommendation V.35. A binary "0" (space) is transmitted when terminal "A" is positive (+.55v +20%) to terminal "B" (-.55V +20%). A binary 1 is transmitted when terminal "A" is negative (-.55v +20%) to terminal "B" (+.55v +20%). The drivers produce a nominal 1.1 volts peak-to-peak signal balanced with respect to ground.

c. Bit Rate/Cable Length.

(1) Maximum Cable Length. The recommended maximum cable length between a V.35 DCE and DTE is 30 feet when overall shielded, low capacitance, twisted pair cable is used. Cable lengths of 100 feet are also possible.

d. Interchange Circuits.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in table 4-1.

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: either the software reacts to the circuit signal when it changes, or the software can assert a circuit when necessary (such as LL which can be used by operations personnel for testing connections). Unsupported circuits either are not read by the software or a value is written to the circuit by the software, and that value does not change during operation. Table 4-1 describes circuit use.

(3) Interchange Circuit Definitions. EIA-232-D signal names are used throughout this chapter.

(a) Signal Ground. See EIA-232-D.

(b) DCE Ready. This circuit must be asserted ON by the DCE, and it is monitored by the PSN software.

(c) Data Set Ready. This circuit must be asserted on by the DCE, and it is monitored by the PSN.

(d) Transmitted Data. See EIA-232-D.

(e) Received Data. See EIA-232-D.

(f) Transmitter Signal Element Timing (DTE Source). See EIA-232-D. Also see subsection 2.b of this guide. This circuit provides the clock for Transmitted Data when the PSN sources timing. The frequency of this circuit should be equal to that of Terminal Receive Timing.

(g) Transmitter Signal Element Timing (DCE Source). See EIA-232-D. This circuit provides the clock for Transmitted Data when the DCE sources timing.

(h) Receiver Signal Element Timing (DCE Source). See EIA-232-D. This circuit provides clock for Received Data when the DCE sources timing.

(i) Request to Send. This circuit is asserted ON by PSN software when the link is initialized.

(j) Clear to Send. This circuit must be asserted ON by the DCE and is monitored by PSN software to determine line status. If the signal state on this line changes to OFF, the software macrocode will stop data transmission.

(k) Received Line Signal Detector. This circuit must be asserted ON by the DCE, and is monitored by PSN software to determine line status. If the signal state on this line changes to OFF, the software macrocode will stop receiving data.

(l) Terminal Receive Timing. This circuit is received by another DTE via a crossover cable when the C/30E sources timing, providing clock for Received Data. The frequency of this circuit should be equal to that of DTE-Sourced Transmitter Signal Element Timing. This circuit is equivalent to DC in older versions of EIA-232, as referenced in chapter 3.

TABLE 4-1. V.35 INTERCHANGE CIRCUIT USE

CCITT ID	Name	Source	Electrical State	Required State of Control/Status Signals	Comments
101	Protective Ground	DTE/DCE	Ground	N/A	
102	Signal Ground	DCE/DTE	Ground	N/A	
103	Transmitted Data	DTE	Active	N/A	Data Circuit
104	Received Data	DCE	Active	N/A	Data Circuit
105	Request to Send	DTE	Active	ON	Asserted ON by
106	Clear to Send	DCE	Active	ON	Asserted ON by monitored by determine lin
107	Data Set Ready	DCE	Active	ON	Asserted ON by monitored by
109	Received Line Signal Detector	DCE	Active	ON	Asserted ON by monitored by PS determine lin
113	Transmitter Signal Element Timing	DTE	Active	N/A	Timing circuit Data when the P timing.
---	Terminal Receive Timing	DTE	Active	N/A	Timing circuit Data when the timing.
114	Transmitter Signal Element Timing	DCE	Active	N/A	Timing circuit Data when the D timing.
115	Receiver Signal Element Timing	DCE	Active	N/A	Timing circuit Data when the D timing.

NOTES: N/A = Not Applicable

3. Mechanical Characteristics. All V.35 connectors offered for the C/30E meet the specifications provided in this section. Cables for this interface, supplied by DDN, are equipped with an EIA-449 connector at one end to mate with the EIA-449 connector on the C/30E fantail; the other end provides a MIL-C-28748 34-pin connector to mate with the V.35 DCE.

a. Interface Connectors. All V.35 connectors on the C/30E fantail are DC-37P type (male) connectors. They are wired as described in table 4-2.

(1) Intermating dimensions are in accordance with EIA-449-D.

(2) The means for C/30E DTE connectors to latch and unlatch from the latching blocks on the DCE connector are within the dimensions specified in EIA-449, section 3.3.1. DDN uses the English 4-40 thread latching block.

b. Connector Contact Assignments. DDN standard node V.35 connector contact assignments are in accordance with CCITT Recommendation V.35 and ISO 2593. Table 4-2 provides DDN V.35 connector pin assignments. The signals are used as specified in section 2.d.3.

4. Interconnecting Cables.

a. For interconnecting cable specifications, see chapter 1, section 4, of this guide.

b. Figure 4-1 is a cabling diagram of a V.35 PSN and nearby V.35 host, and figure 4-2 provides an example of an interconnecting cable (BBNCC P/N# 2409320G01).

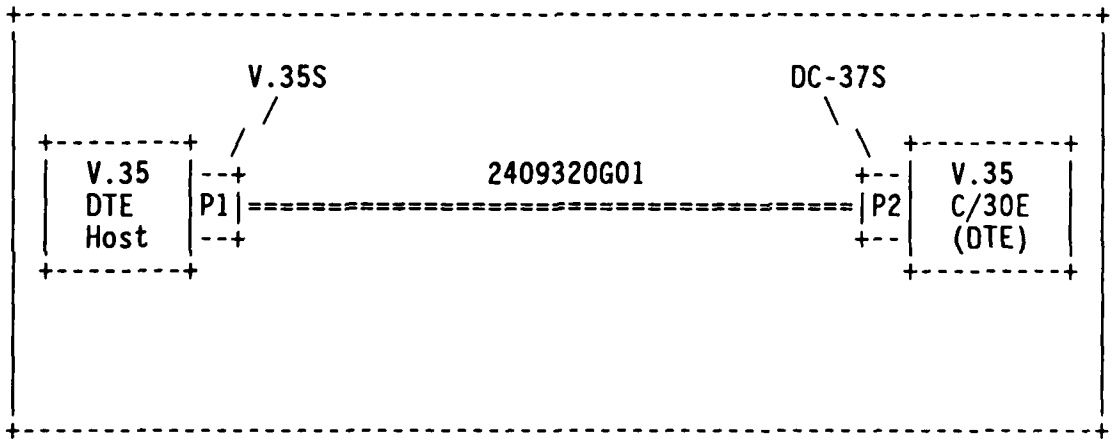


FIGURE 4-1. C/30E PSN AND NEARBY V.35 HOST CABLING DIAGRAM

TABLE 4-2. V.35 34-PIN AND 37-PIN CONNECTOR PINOUT

34-pin #	37-pin* #	CCITT ID	Signal Name	449 Name
A	1	101	Shield	FG
P	4	103	Transmitted Data	SD+
S	22	103	Transmitted Data	SD- **
Y	5	114	Transmitter Signal Element Timing (DCE Source)	ST+
a/AA	23	114	Transmitter Signal Element Timing (DCE Source)	ST-
R	6	104	Received Data	RD+
T	24	104	Received Data	RD-
C	7	105	Request to Send	RS+
-	25	102	Signal Ground	SG
V	8	115	Receiver Signal Element Timing (DCE Source)	RT+
X	26	115	Receiver Signal Element Timing (DCE Source)	RT-
D	9	106	Clear to Send +	CS+
-	27	102	Signal Ground	SG
K	10	141	Local Test Loopback	LL (LT)
E	11	107	Data Set Ready +	DM+
-	29	102	Signal Ground	SG-
-	31	102	Signal Ground	SG-
F	13	109	Received Line Signal Detector	RR
U	17	---	Terminal Timing	TT+ ***
W	35	---	Terminal Timing	TT- ***
L	16	---	Terminal Receive Timing	TRT+ ***
N	34	---	Terminal Receive Timing	TRT- ***
B	19	102	Signal Ground	SG
B	37	102	Signal Ground	SG

* This information represents a straight cable to a V.35 DCE.
** The + and - symbols, used in EIA-449, correspond to A and B, respectively, in V.35 terminology.
*** Internally generated clocks are supplied on pins TT and TRT.

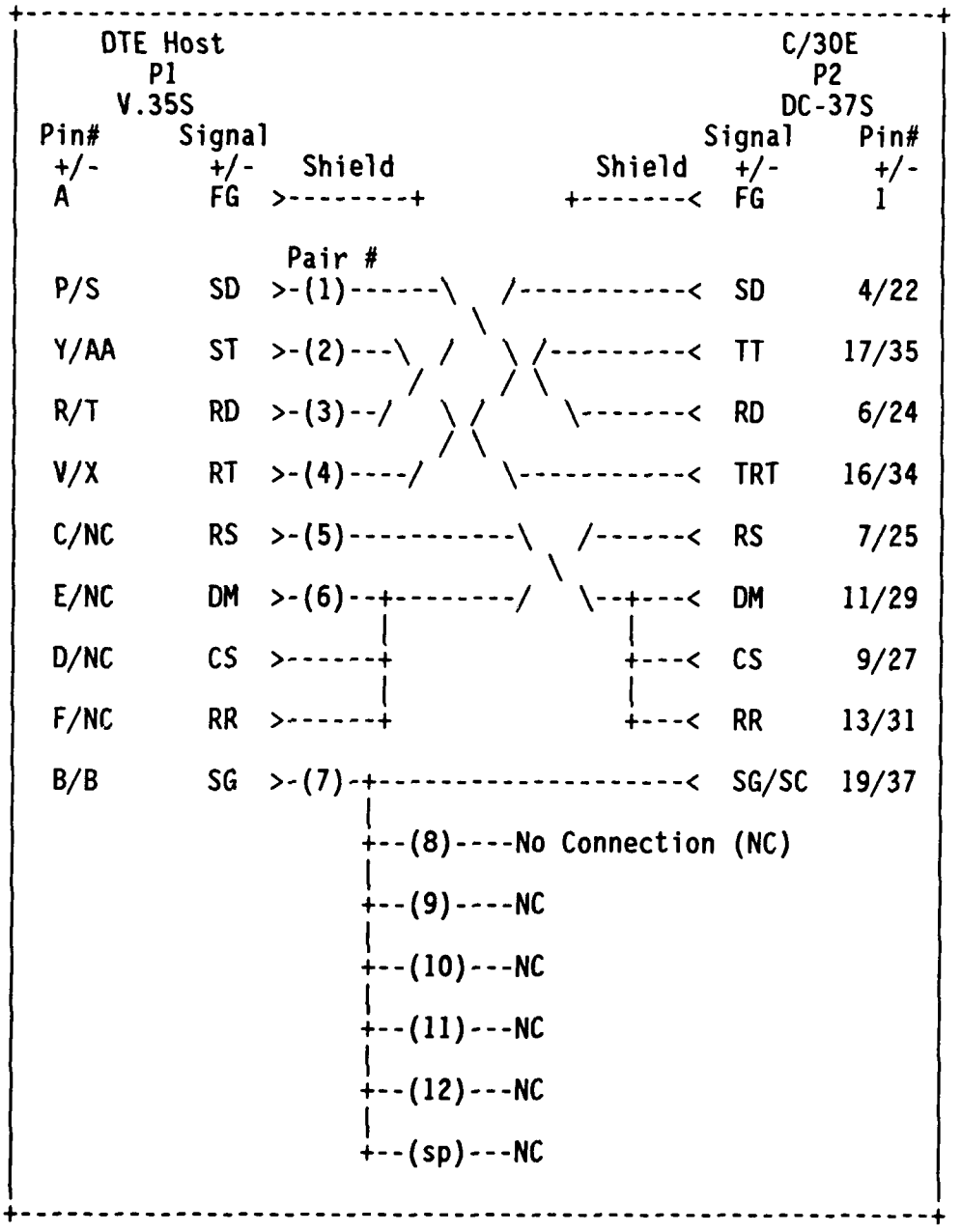


FIGURE 4-2. CABLE EXAMPLE: C/30E PSN TO NEARBY V.35 HOST

CHAPTER 5. MIL-STD-188-114 NEIGHBOR OR NEARBY TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the MIL-STD-188-114 balanced DTE interface that connects the C/30E PSN with a modem. DDN supports Extended Modem Looping (XMOD) through the MIL-STD-188-114 interface. This interface is largely in conformance with the EIA-Standard 449/422, considered the general commercial equivalent to MIL-STD-188-114. For ease of reference, Table 5-1 equates the EIA-449, EIA-232-D, and CCITT interface signal names. However, in the rest of chapters 5 and 6, only the EIA-449 signal names will be used.

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E 188-114 interface circuits are in accordance with MIL-STD-188-114, chapter 5, except with regard to subsection 5.1.1.3: Open Circuit Measurement. The C/30E open circuit driver voltage, measured in accordance with 5.1.1.3, is less than $\pm$9.0V for balanced drivers and $\pm$4.5V for unbalanced drivers.

b. Clocking. Two fantails, MMB and MMBC, provide the EIA-449 connectors that terminate cables from all I/O interfaces. The MMB fantail connector is configured as a DTE. When the MMB fantail is used, the DCE must provide clock because the MMB fantail does not support clock-sourcing capability. The MMBC, a clock-sourcing enhanced fantail, is configured as a DCE and can provide clock.

(1) MMBC Clock Rates. MMBC and MMB interface hardware support any external clock between 1.2 kb/s and 112 kb/s. However, DDN policy is that the minimum PSN bit rate be 9.6 kb/s. When MMBC clock-sourcing capability is used, the MMBC on-board clock generator provides the frequencies described in Table 5-2.

TABLE 5-2. FREQUENCIES PROVIDED BY THE MMBC FANTAIL

Clock Frequency	Accuracy*
112kHz, 64kHz, 56kHz, 50kHz	$\pm$0.005% (50 ppm**)

* Accuracy over a temperature range of 10 to 30 degrees C.
** PPM = Parts Per Million

TABLE 5-1. SIGNAL NAME EQUIVALENCY TABLE

EIA-449 ID	Name	EIA-232-D ID	Name	CCITT ID	Nam
SG	Signal Ground	AB	Signal Ground	102	S
SC	Send Common	--		102a	D
RC	Receive Common	--		102b	D
SD	Send Data	BA	Transmitted Data	103	T
RD	Receive Data	BB	Received Data	104	R
RS	Request To Send	CA	Request To Send	105	R
CS	Clear To Send	CB	Clear To Send	106	R
DM	Data Mode	CC	Data Set Ready (DCE Ready)	107	D
TR	Terminal Ready	CD	Data Terminal Ready (DTE Ready)	108/2	D
RR	Receiver Ready	CF	Received Line Signal Detector	109	D
IS	Terminal In Service	--		---	
SR	Signaling Rate Selector	CH	Data Signal Rate Selector (DTE Source)	111	D
SI	Signaling Rate Indicator	CI	Data Signal Rate Selector (DCE Source)	112	D
NS	New Signal	--		---	
TT	Terminal Timing	DA	Transmitter Signal Element Timing (DTE Source)	113	T
ST	Send Timing	DB	Transmitter Signal Element Timing (DCE Source)	114	T
RT	Receive Timing	DD	Receiver Signal Element Timing	115	R
SS	Select Standby	--		116	S
SF	Select Frequency	--		126	S
LL	Local Loopback	LL	Local Loopback	141	L
RL	Remote Loopback	RL	Remote Loopback	140	R

(2) Signaling Sense. Signaling sense for balanced and unbalanced circuits is in accordance with EIA-422-A with the exception that the differential voltage applied to the interconnecting cable is in the range of 2 volts to 9 volts for the C/30E. As defined in EIA-422-A, ON (0, Space, or +) is generated when A terminal is positive with respect to the B terminal, and OFF (1, MARK, or -) is generated when A terminal is negative with respect to the B terminal.

(3) On-Board Jumpers. There are three jumper option pairs on the MMB:

--1 Used for RS-422 mode (balanced Category I circuits)
--2 Used for RS-423 mode (unbalanced Category I circuits)
--3 Used for normal (univerted) data operation
--4 Used to invert transmit and receive data
--5 Used for invert data in RS-423 mode
--6 Used for RS-422 mode or normal data in RS-423 mode

Boards are shipped from the factory with steps 1, 3, 6 selected.

c. Bit Rate and Cable Length. Interconnecting cable length and its relation to data signaling rates are in accordance with EIA Standard 449, section 6.10, and EIA Standard 422-A, section 4.3 and the appendix.

(1) Maximum Cable Length. The maximum length of the cable is 1000 feet.

(2) Slew Rate Limiting. Signal rise time is set to 1 microsecond (100 kb/s value).

d. Interchange Circuits. There are two EIA-449 trunk interfaces: a non-clock-sourcing interface provided by the MMB daughterboard, and a clock-sourcing interface provided by the MMBC daughterboard. The difference in the implementation of these two interfaces is described in this section, as well as in tables 5-3 and 5-4.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in Tables 5-3 and 5-4.

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: the software can react to a received signal when it changes, and the software can assert a transmitted signal when necessary (such as RS, TR, and LL which can be used by operations personnel for testing connections). Unsupported circuits are either not read by the software or a value is written to the circuit by the software and that value does not change during operation. Tables 5-3 and 5-4 provides a list of circuits and their use.

(3) Interchange Circuit Definitions. For additional information about these interchange circuits, see EIA Standard 449. The following descriptions assume use of full period/full duplex circuits, with flow control handled at higher levels.

(a) Signal Ground. See EIA Standard EIA-449.

(b) Send Common. See EIA Standard EIA-449.

(c) Receive Common. See EIA Standard EIA-449.

(d) Terminal in Service. For the non-clock-sourcing interface, IS is tied ON by the hardware. For the clock-sourcing interface, this circuit is not connected.

(e) Incoming Call. IC is not connected.

(f) Terminal Ready. For the non-clock-sourcing interface, TR is asserted OFF by PSN software when the link is initialized and allows Monitoring Center control. For the clock-sourcing interface, TR is not connected.

(g) Data Mode. For the non-clock-sourcing interface, DM is not monitored by the PSN software. For the clock-sourcing interface, DM is asserted ON by hardware.

(h) Send Data. See EIA Standard EIA-449.

(i) Receive Data. See EIA Standard EIA-449.

(j) Terminal Timing. See EIA Standard EIA-449. TT is supported as a "reflected clock" in phase with ST.

(k) Send Timing. See EIA Standard EIA-449.

(l) Receive Timing. See EIA Standard EIA-449.

(m) Request to Send. For the non-clock-sourcing interface, RS is asserted OFF by the PSN software when the link is initialized. RS allows Monitoring Center control. For the clock-sourcing interface, RS is not connected.

(n) Clear to Send. For the non-clock-sourcing interface, CS is not monitored by the PSN software. For the clock-sourcing interface, CS is asserted ON by hardware.

(o) Receiver Ready. For the non-clock-sourcing interface, RR is not monitored by PSN software. For the clock-sourcing interface, RR is asserted ON by hardware.

(p) New Signal. For the non-clock-sourcing interface, NS is tied OFF by the hardware. For the clock-sourcing interface, NS is not connected.

(q) Select Frequency. For the non-clock-sourcing interface, SF/SR is electrically active and asserted OFF by the hardware when the link is initialized. For the clock-sourcing interface, SF/SR is not connected.

(r) Signaling Rate Selector. See Select Frequency, 2.d.3.q above for a description.

(s) Signaling Rate Indicator. SI is not connected.

(t) Local Loopback. For the non-clock-sourcing interfaces, LL is electrically active, but asserted OFF by PSN software when the link is initialized. LL can be controlled by the Monitoring Center. For the clock-sourcing interface, LL is not connected.

(u) Remote Loopback. RL is electrically active, but asserted OFF by PSN software when the link is initialized. For the non-clock-sourcing interface, RL is not available for Monitoring Center control. For the clock-sourcing interface, RL is asserted when another DCE requests the PSN to enter remote loopback.

(v) Test Mode. For the non-clock-sourcing interface, TM is not connected. For the clock-sourcing interface, TM is OFF during normal operations but ON during loopback operations to acknowledge the loopback request from another DCE.

(w) Select Standby. For the non-clock-sourcing interface, SS is tied OFF by hardware. For the clock-sourcing interface, SS is not monitored by PSN software but it is used as the remote loop indicator when the PSN requests another DCE to enter remote loopback.

(x) Standby Indicator. For the non-clock-sourcing interface, SB is not connected. For the clock-sourcing interface, SB is OFF during normal operations, and it is used as the remote loop request signal for loopback operations when the PSN requests another DCE to enter remote loopback.

TABLE 5-3. DDN STANDARD NODE MMB*/MMBC INTERCHANGE CIRCUIT USE

449 ID	EIA-449 Name	Source	Electrical Circuit	Required State of Control/Status Signals	Comments
SG	Signal Ground	DTE/DCE	Ground	N/A	Gr
SC	Send Common	DTE	Ground	N/A	Co
RC	Receive Common	DCE	Ground	N/A	Co
SD	Send Data	DTE	Active	N/A	Da
RD	Receive Data	DCE	Active	N/A	Da
RS	Request to Send	DTE	Active	OFF	As T
CS	Clear to Send	DCE	Active	Don't Care	No
DM	Data Mode	DCE	Active	Don't Care	No
TR	Terminal Ready	DTE	Active	OFF	As T
RR	Receiver Ready	DCE	Active	Don't Care	No
SQ	Signal Quality	DCE	Not Connected	Don't Care	No
SF/SR	Select Frequency/ Signaling Rate Sel.	DTE	Static	OFF	Ti
SI	Signaling Rate	DCE	Not Connected	Don't Care	No
TT	Terminal Timing	DTE	Active	N/A	Ti Da
ST	Send Timing	DCE	Active	N/A	Ti Da
RT	Receive Timing	DCE	Active	N/A	Ti Da
SS	Select Standby	DTE	Static	OFF	Ti
SB	Standby Indicator	DCE	Not Connected	Don't Care	No
IC	Incoming Call	DCE	Not Connected	Don't Care	No
LL	Local Loopback	DTE	Active	OFF	Ti T
RL	Remote Loopback	DTE	Static	OFF	Ti
TM	Test Mode	DCE	Not Connected	Don't Care	No
NS	New Signal	DTE	Static	OFF	Ti
IS	Terminal in Service	DTE	Static	ON	Ti
AT	Alternate Timing	DTE	Not Connected	N/A	No

NOTE: N/A = Not Applicable
* MMB provides a non-clock-sourcing (DTE) interface.

3. Mechanical Characteristics. All EIA-449/422 connectors offered for the C/30E meet the following specifications.

a. Interface Connectors. All C/30E EIA-449 connectors interfacing an MMB with an MMBC have DC-37P type (male) connectors for the MMB side and a DC-37S type (female) connectors for the MMBC side. Two interfacing MMBC-configured PSNs use two DC-37P connectors.

(1) Intermating dimensions are in accordance with EIA-449, section 3.3.1.

(2) The means for C/30E DTE connectors to latch and unlatch from the latching blocks on the DCE connector are within the dimensions specified in EIA-449, section 3.3.2. DDN uses the English 4-40 thread latching block.

b. Connector Contact Assignments. All C/30E EIA-449/422 contact assignments are in accordance with EIA-449, section 3.4. Table 5-4 provides the DDN standard node connector pinout. The signals are used as specified in section 2.d.3 of the Standard.

4. Interconnecting Cables.

a. For interconnecting cable specifications, see chapter 1, section 4, of this guide.

b. Figure 5-1 is a cabling diagram of a C/30E PSN connected to a nearby EIA-449 PSN via an MMB-MMBC configuration. Figure 5-2 is a cabling diagram of a C/30E PSN connected to a nearby EIA-449 PSN via an MMBC-MMBC configuration, the preferred configuration for the DDN. Figure 5-3 is an example of a cable used to interconnect the MMB-MMBC configuration, whereas figure 5-4 illustrates the MMBC-MMBC nearby EIA-449 PSN connection.

(1) Conductor Size. Interconnecting cables should be in accordance with MIL-STD-188-114, Appendix C, with regard to conductor size (subsection 30.3.1). Interconnecting cables or wires should be composed of wires of a 24 AWG or larger conductor for solid or stranded copper wires, or for non-copper conductors a sufficient size to yield a dc wire resistance not to exceed 30 ohms/1000 feet per conductor.

(2) Mutual Pair Capacitance. In accordance with MIL-STD-188-114, the capacitance between one wire in the pair to the other wire in the pair should not exceed 20 picofarads/foot, and the value should be reasonably uniform over the length of the wire or cable.

(3) Stray Capacitance. In accordance with MIL-STD-188-144, the capacitance between ome wire in the cable to all others in the cable sheath, with all others connected to ground, should not exceed 40 picofarads/foot, and should be reasonably uniform for a given conductor over the length of the wire or cable.

TABLE 5-4. DDN STANDARD NODE EIA-449 (DTE) CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
1	FG		Frame Ground
2	SI	111	Not Connected
20	RC	102b	Receive Common
3	AT	---	Not Connected
21	AT	---	Not Connected
4	SD	103	Send Data +
22	SD	103	Send Data -
5	ST	114	Send Timing +
23	ST	114	Send Timing -
6	RD	104	Receive Data +
24	RD	104	Receive Data -
7	RS	105	Request to Send +
25	RS	105	Request to Send -
8	RT	115	Receive Timing +
26	RT	115	Receive Timing -
9	CS	106	Clear to Send +
27	CS	106	Clear to Send -
10	LL	141	Local Loopback
28	IS	---	Tied to "1" on MMB, Not Connected on MMBC
11	DM	107	Data Mode +
29	DM	107	Data Mode -
12	TR	108.2	Terminal Ready +
30	TR	108.2	Terminal Ready -
13	RR	109	Receiver Ready +
31	RR	109	Receiver Ready
14	RL	140	Remote Loopback - Tied to "0" on MMB, Active on MMBC
32	SS	116	Select Standby - Tied to "0"
15	IC	125	Incoming Call
33	SQ	110	Signal Quality
16	SF/SR	126	Select Frequency/Signaling Rate Tied to "1"
34	NS	---	New Signal - Tied to "0"
17	TT	113	Terminal Timing +
35	TT	113	Terminal Timing -
18	TM	142	Not Connected - MMBC Has This
36	SB	117	Not Connected - MMBC Has This
19	SG	102	Signal Ground
37	SC	102a	Send Common

(4) Pair-to-Pair Balanced Crosstalk. In accordance with MIL-STD-188-144, Appendix C, with regard to pair-to-pair balanced crosstalk (subsection 30.3.4), the crosstalk from one pair of wires to any other pair in the same cable sheath should have a minimum value of 40 dB attenuation measured at 150 kHz.

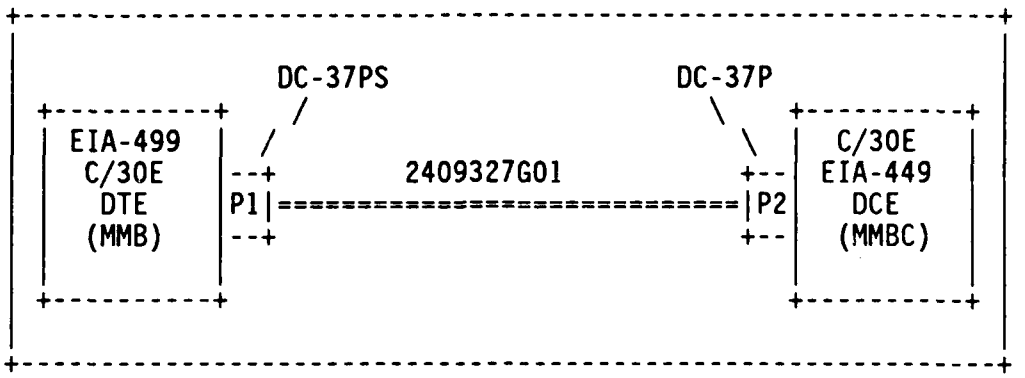


FIGURE 5-1. C/30E EIA-449 PSN AND NEARBY EIA-449 PSN CABLING DIAGRAM (C/30E SOURCES CLOCK)

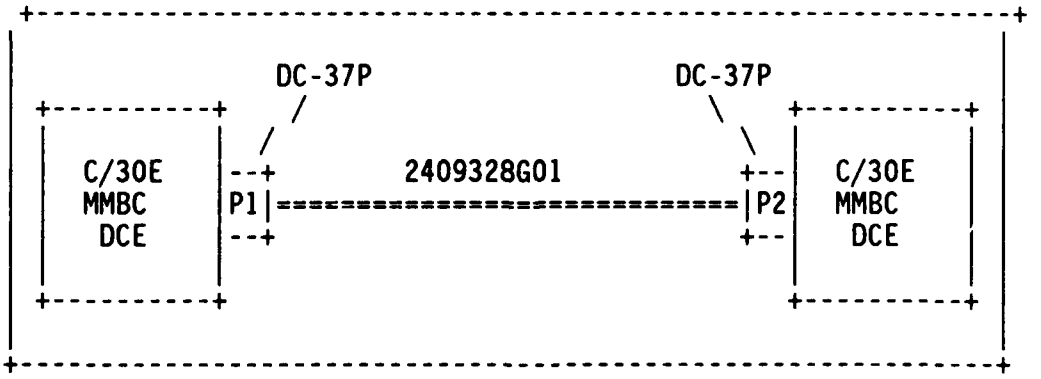


FIGURE 5-2. C/30E PSN WITH MMBC TO EIA-449 NEARBY PSN CABLING DIAGRAM WITH MMBC (C/30E SOURCES CLOCK)

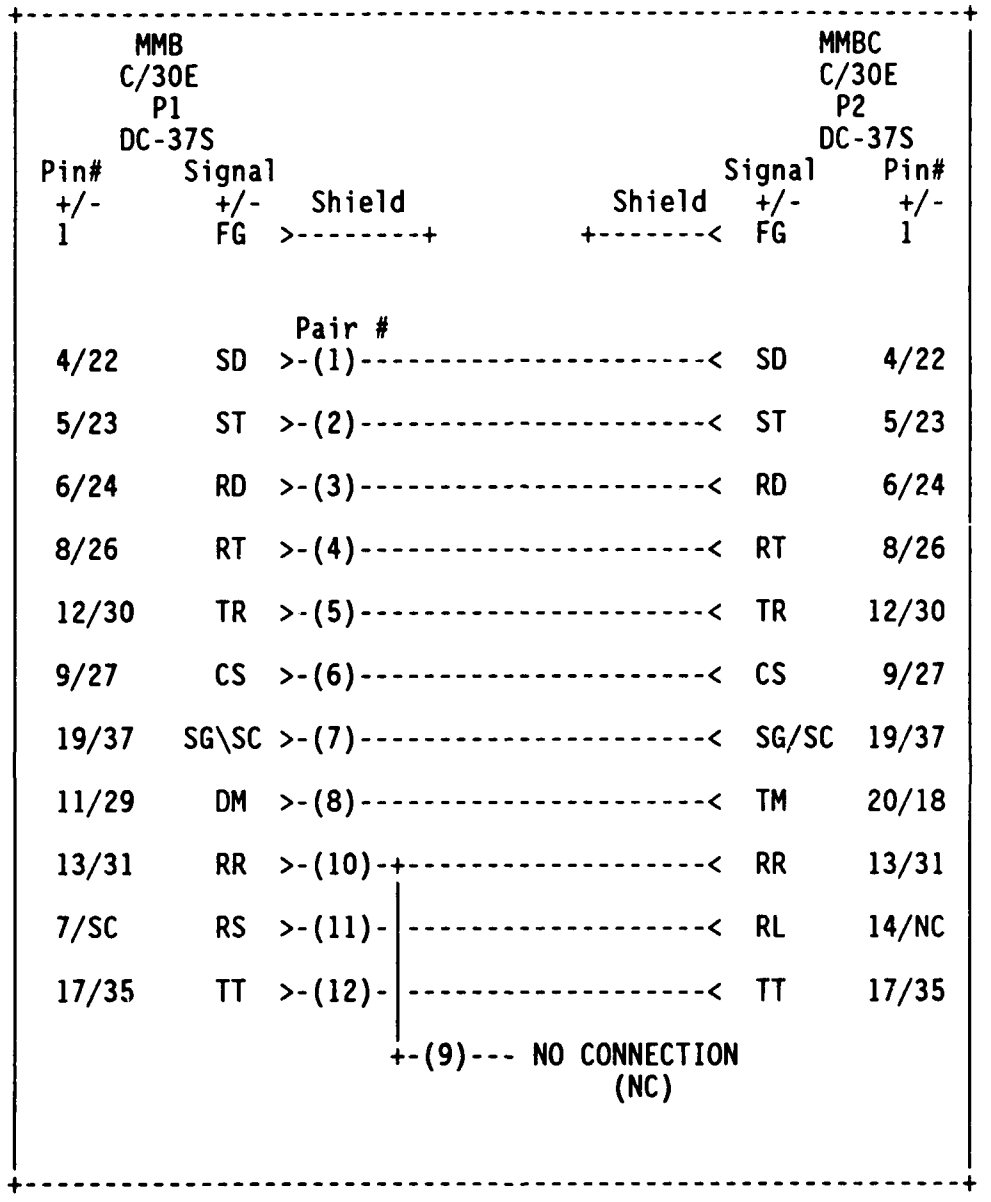


FIGURE 5-3. CABLING EXAMPLE: C/30E WITH MMB TO EIA-449 NEARBY PSN WITH MMBC (C/30E SOURCES CLOCK)

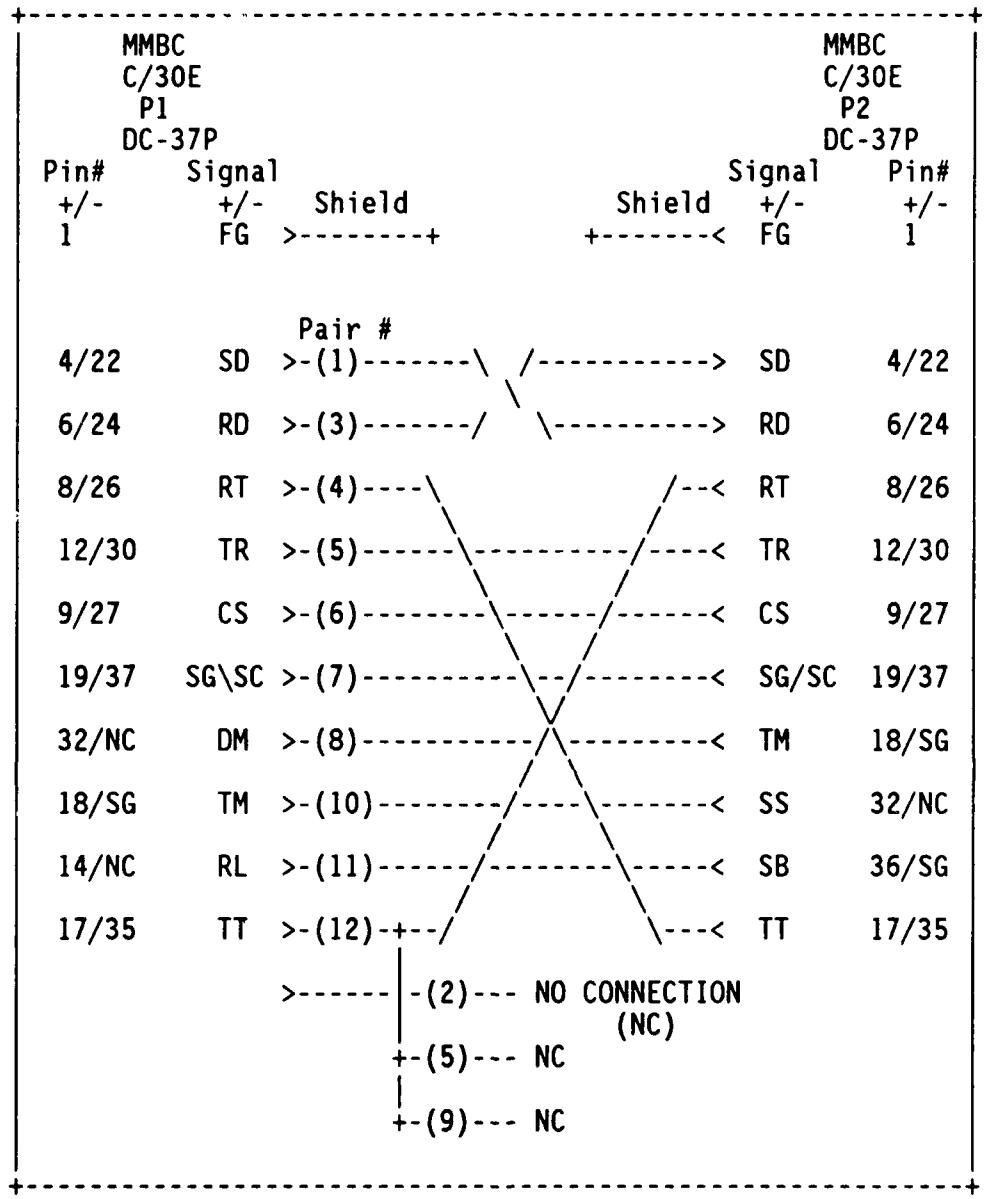


FIGURE 5-4. CABLING EXAMPLE: C/30E WITH MMBC TO EIA-449 NEARBY PSN WITH MMBC (C/30E SOURCES CLOCK)

CHAPTER 6. MIL-STD-188-114 REMOTE TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the MIL-STD-188-114 balanced remote trunk interface. DDN supports Extended Modem Looping (XMOD) through the MIL-STD-188-114 interface. This chapter also documents the interface between the remote modem and the PSN (demarcation point A in figure 6-1) with no intervening cryptographic devices (KG-84As). Eventually KG-84As will be required for all trunk circuits; therefore, chapter 6 also provides an example of the cabling that connects from the remote modem to the remote Fixed Plant Adapter (FPA) and then to the PSN (demarcation point B in figure 6-2).

2. Electrical Characteristics.

a. Voltage Levels. The modems used will conform to EIA Standard 449. The electrical interface of the KG-84A is in accordance with MIL-STD-188-114, chapter 5, except with regard to subsection 5.1.1.3: Open Circuit Measurement. The open circuit driver voltage, measured in accordance with section 5.1.1.3 of this statement, is less than $\pm$9.0V for balanced drivers and $\pm$4.50V for unbalanced drivers.

b. Clocking.

(1) Modem Clocking. The modem supplies timing on the Send Timing and Receive Timing circuits. Terminal Timing isnot supported for remote PSN interfaces. While the DDN hardware will support between 1.2 kb/s and 64 kb/s, DDN policy states that the minimum PSN access rate be 9.6 kb/s.

(2) Signaling Sense. Signaling sense for balanced and unbalanced circuits is in accordance with EIA Standard 422-A with the exception of the differential voltage, which applied to the interconnecting cable, is in the C/30E range of 2 volts to 9 volts. As defined in EIA Standard 422-A, ON (0, Space, or +) is generated when the A terminal is positive with respect to the B terminal, and OFF (1, MARK, or -) is generated when the A terminal is negative with respect to the B terminal.

c. Bit Rate and Cable Length.

(1) EIA-449 Compliance. Interconnecting cable length and its relation to data signaling rates are in accordance with EIA Standard 449, section 6.10, and EIA Standard 422-A, section 4.3 and the Appendix.

(2) Maximum Cable Length. The maximum cable length between the remote modem and the PSN, including the intervening FPA is 1000 feet; however, cable lengths less than 200 feet are preferred.

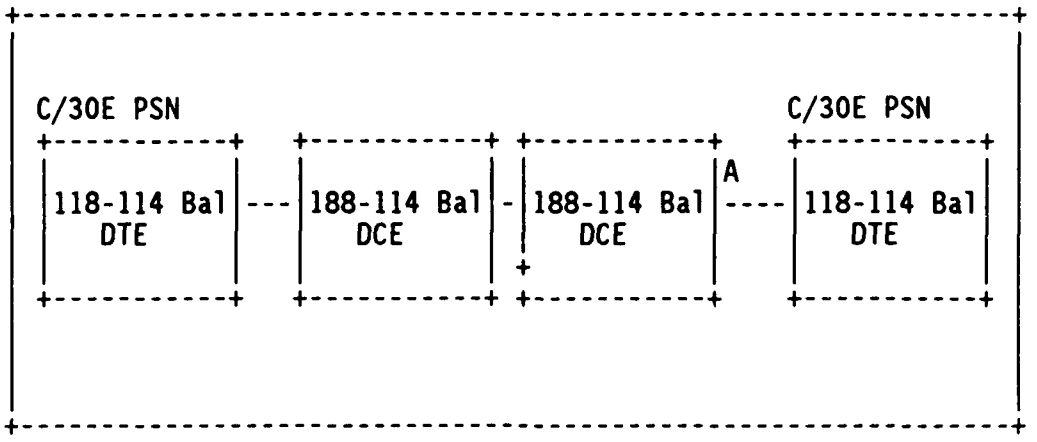


FIGURE 6-1. DEMARCATION POINT "A" BETWEEN THE C/30E AND REMOTE C/30E

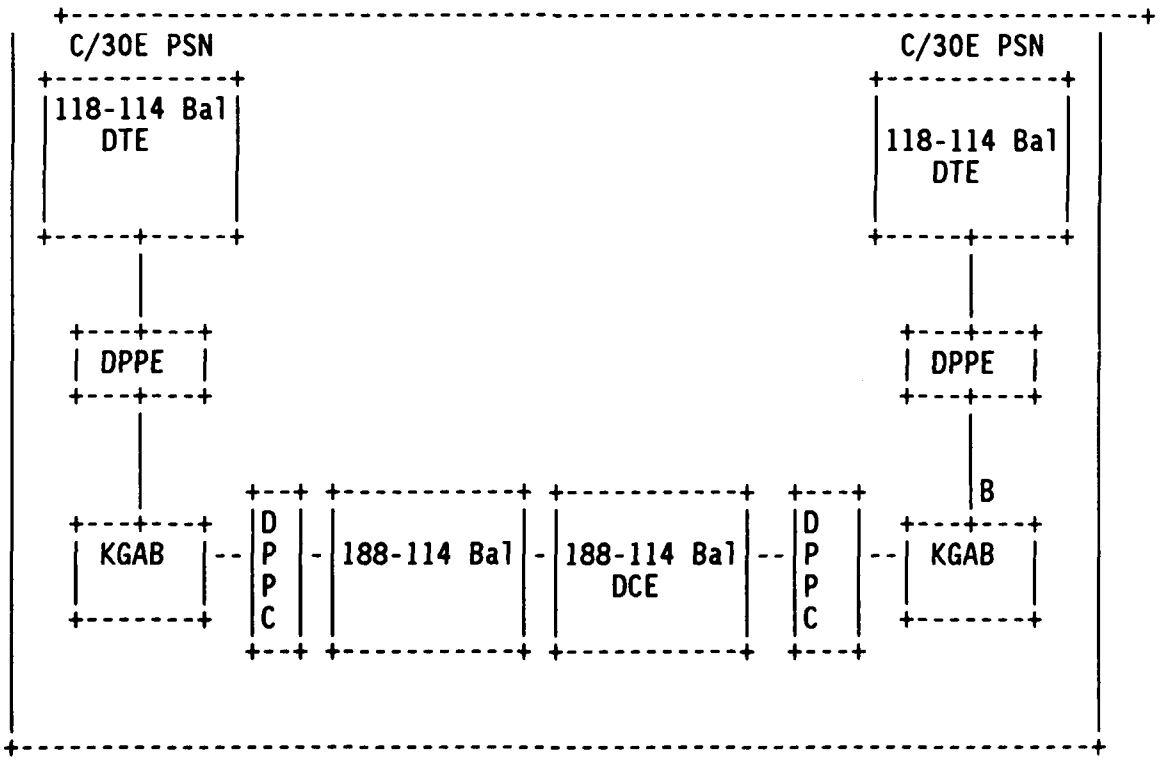


FIGURE 6-2. DEMARCATION POINT "B" BETWEEN THE KGAB AND C/30E PSN

d. Interchange Circuits.

(1) C/30E Local Modem Interface.

(a) Signal flow between the C/30E and the local modem is shown in figure 6-3. This interface and associated hardware are provided by DDN. The signal flow is the same when a KG-84A is used. This interface uses EIA-449 pin assignments.

(b) As shown in figure 6-3, the supported signals are Send Data (SD), Send Timing (ST), Receive Data (RD), and Receive Timing (RT). Clear to Send (CS), Data Mode (DM), and ReceiverReady (RR) are tied ON by the cable connected to the fantail.Terminal Ready (TR) is being used for the Remote Loopback (RL) function. Request to Send (RS) is being used for the Local Loopback (LL) function. The signal LL is being used for the COMSEC Loopback (CL) described below.

(c) A special DDN-specific loopback signal, CL, is provided as shown in figure 6-3. The Local Loopback (LL) signal is used by the PSN to loop the local KG-84A and is designated as "C" loop or CL (standing for COMSEC Loopback) in figure 6-3 after it leaves the C/30E fantail.

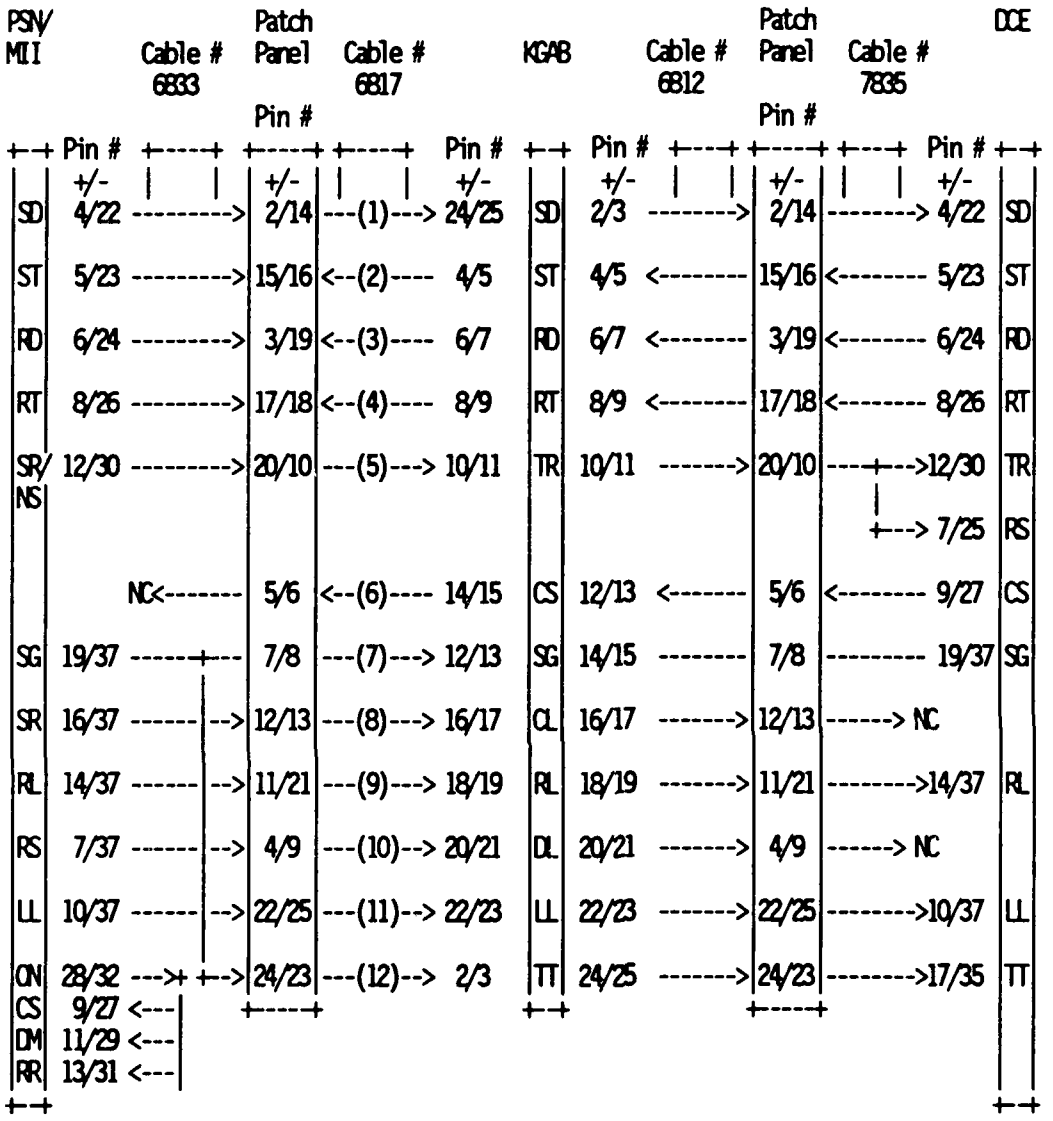
3. Mechanical Characteristics. All EIA-449/422 connectors offered for the C/30E meet the specifications of this section.

a. Interface Connectors. DDN MIL-STD-188-114 DCE connectors are DC-37S type (female) and DC-37P type (male) connectors. The DDN FPA uses an MS connector on the KGAB counter assemblies.

b. Connector Contact Assignments.

(1) C/30E Connectors. All DDN EIA-449/422 contact assignments are in accordance with EIA Standard 449, section 3.4. In chapter 1, Table 5-4 provides the standard DTE pinouts and section 2.d.3 of the Standard provides circuit descriptions.

(2) KGAB Connectors. KGAB connectors to the remote C/30E and the remote modem are shown in Tables 6-2 and 6-3, respectively.



Notes: 1. Pin numbers are the same on both sides of Patch Panel.
2. Encircled numbers are the cable pair numbers.

FIGURE 6-3. FUNCTIONAL SIGNAL FLOW BETWEEN A NEARBY MODEM AND C/30E, OR A SR(ON) NS(OFF) KGAB AND A REMOTE PSN

TABLE 6-1. REMOTE-MODEM DCE INTERFACE CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
4	SD +	103	Send Data
22	SD -	103	Send Data
5	ST +	114	Send Timing
23	ST -	114	Send Timing
6	RD +	104	Receive Data
24	RD -	104	Receive Data
7	RS +	105	Request to Send
25	RS -	105	Request to Send
8	RT +	115	Receive Timing
26	RT -	115	Receive Timing
9	CS +	106	Clear to Send
27	CS -	106	Clear to Send
12	TR +	108.2	Terminal Ready
30	TR -	108.2	Terminal Ready
17	TT +	113	Terminal Timing
35	TT -	113	Terminal Timing
19	SG	102	Signal Ground
37	SC	102a	Send Common
Optional			
2	SI	112	Signaling Rate Indicator
10	LL	141	Local Loopback
11	DM +	107	Data Mode
13	RR	109	Receiver Ready
14	RL	140	Remote Loopback
15	IC	125	Incoming Call
16	SF/SR	126/111	Select Frequency/Signaling Rate Selector
18	TM	142	Test Mode
20	RC	102b	Receive Common
28	IS	---	Terminal In Service
29	DM -	107	Data Mode
31	RR -	109	Receiver Ready
32	SS	116	Select Standby
33	SQ	110	Signal Quality
34	NS	---	New Signal
36	SB	117	Standby Indicator

TABLE 6-2. KGAB - REMOTE C/30E CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
24	SD +	103	Send Data
25	SD -	103	Send Data
4	ST +	114	Send Timing
5	ST -	114	Send Timing
6	RD +	104	Receive Data
7	RD -	104	Receive Data
8	RT +	115	Receive Timing
9	RT -	115	Receive Timing
10	TR +	108.2	Terminal Ready
11	TR -	108.2	Terminal Ready
12	SG	102	Signal Ground
13	SC	102a	Send Common
19	SS	116	Select Standby
Optional			
14	CS +	106	Clear to Send
15	CS -	106	Clear to Send
22	LL	141	Local Loopback
20	DL +	105	"D" Loop (Reserved)
21	DL -	105	"D" Loop (Reserved)
18	RL	140	Remote Loopback
2	TT +	113	Terminal Timing
3	TT -	113	Terminal Timing
16	CL +	126	"C" Loop (KG-84A Loop)
17	CL -	126	"C" Loop (KG-84A Loop)

TABLE 6-3 KGAB - REMOTE MODEM CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
2	SD +	103	Send Data
3	SD -	103	Send Data
4	ST +	114	Send Timing
5	ST -	114	Send Timing
6	RD +	104	Receive Data
7	RD -	104	Receive Data
8	RT +	115	Receive Timing
9	RT -	115	Receive Timing
10	TR +	108.2	Terminal Ready
11	TR -	108.2	Terminal Ready
14	SG	102	Signal Ground
15	SG	102	Signal Ground
24	TT +	113	Terminal Timing
25	TT -	113	Terminal Timing
Optional			
12	CS +	106	Clear To Send
13	CS -	106	Clear To Send
16	CL	---	"C" Loop (KG-84A Loop)
17	CL -	---	"C" Loop (KG-84A Loop)
18	RL +	140	Remote Loopback
19	RL -	140	Remote Loopback
20	DL +	---	"D" Loop (Reserved)
21	DL -	---	"D" Loop (Reserved)
22	LL +	141	Local Loopback
23	LL -	141	Local Loopback

4. Interconnecting Cables. Figures 6-4 and 6-5 provide a cabling diagram of a configuration with a C/30E, modems, and FPAs. Table 6-4 describes the cables used for interconnecting these devices. See chapter 1, section 4, for specifications on interconnecting cables.

TABLE 6-4. REMOTE INTERFACE CABLES

Connection	BBNCC P/N#	Description
PSN IMP/MII to DPPE	2406833G01	12-pr, PSN/MSYNC 188-114 Bal Host to DB25P
DPPE to KGAB	2406817G01	12-pr, DB25S to FPA-J1
KGAB to DPPC	2406812G01	12-pr, FPA-J2 to DB25P
DPPC to DCE	2407835G01	12-pr, DB25S to 188-114 DCE

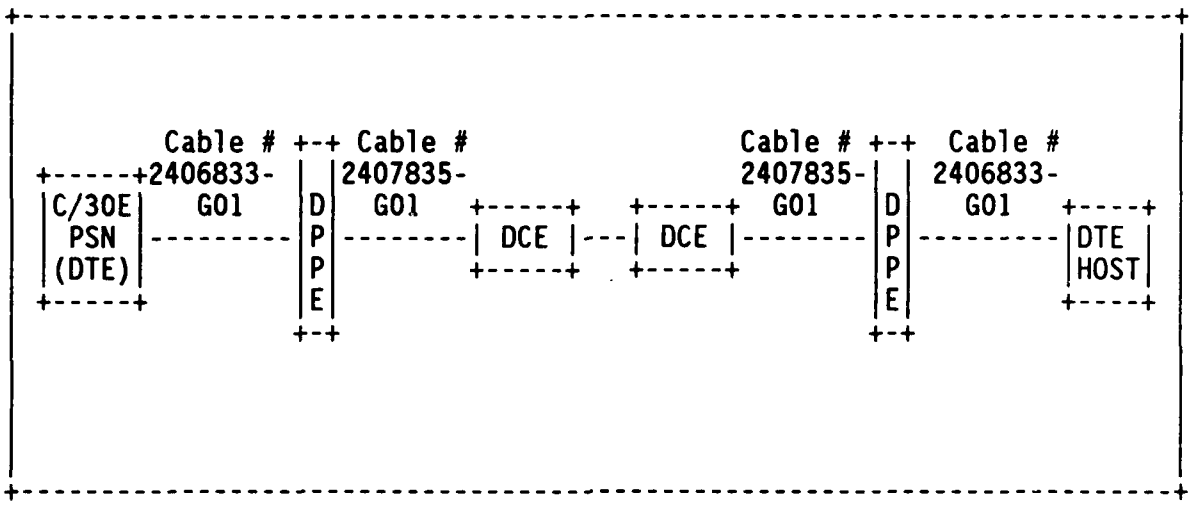


FIGURE 6-4. C/30E AND REMOTE HOST CABLING DIAGRAM

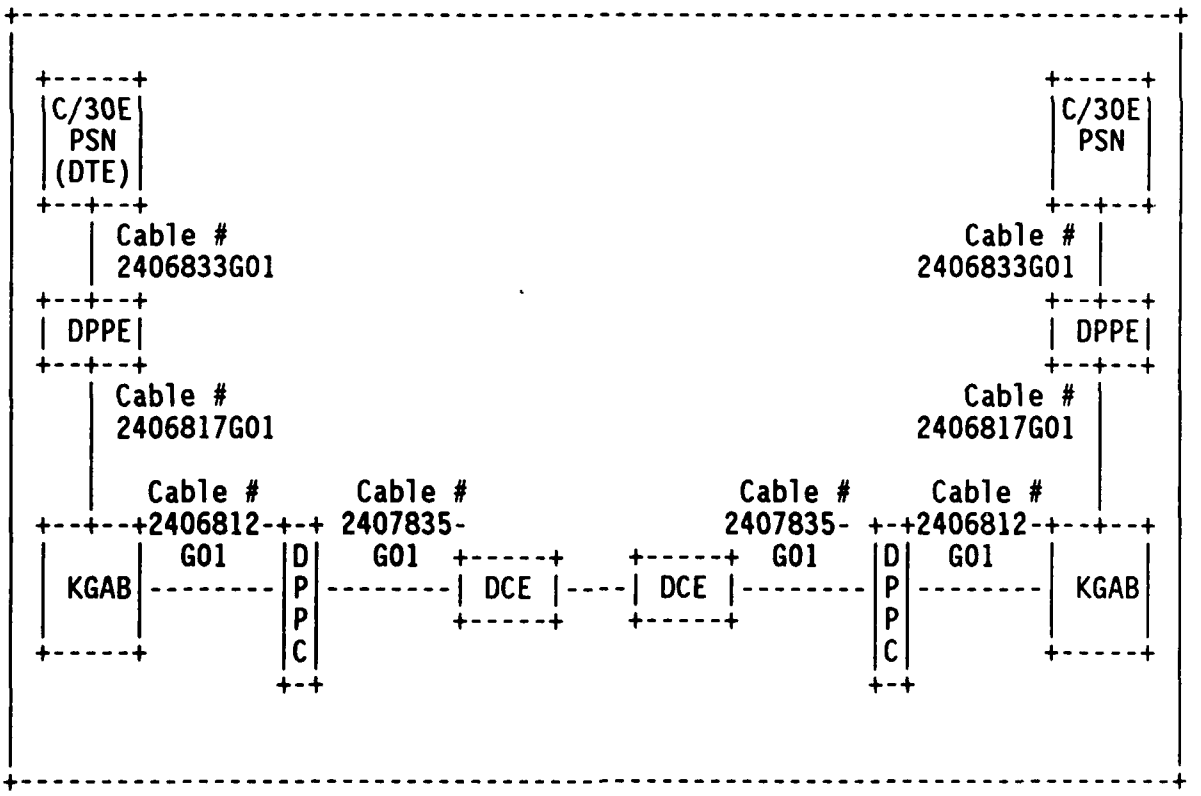


FIGURE 6-5. C/30E AND REMOTE TRUNK CABLING DIAGRAM
(WITH CRYPTOGRAPHIC DEVICES)

CHAPTER 7. EIA-232-D NEIGHBOR OR NEARBY TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the obsolete DDN EIA-232-D PSN connection at the neighbor or nearby PSN. DDN supports Extended Modem Looping (XMOD) through the EIA-232-D interface. For ease of reference, Table 7-1 equates the EIA-232-D, EIA-449, and CCITT interface signal names. However, in the rest of this chapter, only the EIA-232-D signal name will be used. DDN uses the EIA-232-D interface only where an existing non-DDN standard PSN provides such an interface, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN standard (MIL-STD-188-114 balanced serial trunk interfaces).

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E EIA-232-D interface circuits are in accordance with EIA Standard 232-D, section 2.1. For normal operation, the open circuit driver voltage shall be no more than $\pm$15 V.

b. Clocking.

(1) Supported Clock Rates. The MMR fantail contains the connector that terminate cables from all I/O interfaces. The fantail contains one EIA-232-D connector configured as a DTE. This interface has no clock-sourcing capability. The hardware can support external clock rates between 1.2 kb/s and 112 kb/s. However, DDN policy is 9.6 kb/s for the minimum PSN bit rate and 19.2 kb/s for the maximum rate.

(2) Signaling Sense. Signaling sense is in accordance with EIA Standard 232-D, subsection 2.1.3. The signal is considered marking (OFF) when the voltage on the interchange circuit is more negative than -3 V with respect to signal ground, and spacing (ON) when the voltage is more positive than +3 V with respect to signal ground.

c. Bit Rate and Cable Length. Interconnecting cable length is in accordance with EIA-232-D, section 3.1. The recommended maximum cable length between an EIA-232-D DCE and DTE is 200 feet when overall shielded, low capacitance, twisted pair cable is used.

d. Interchange Circuits.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in Table 7-2.

TABLE 7-1. SIGNAL NAME EQUIVALENCY TABLE

EIA-232-D ID	Name	EIA-449 ID	Name	CCITT ID	Name
AB	Signal Ground	SG	Signal Ground	102	S
CE	Ring Indicator	IC	Incoming Call	125	C
CD	DTE Ready	TR	Terminal Ready	108/2	D
CC	DCE Ready	DM	Data Mode	107	D
BA	Transmitted Data	SD	Send Data	103	T
BB	Received Data	RD	Receive Data	104	R
DA	Transmitter Signal Element Timing (DTE Source)	TT	Terminal Timing	113	T
DB	Transmitter Signal Element Timing (DCE Source)	ST	Send Timing	114	T
DD	Receiver Signal Element Timing (DCE Source)	RT	Receive Timing	115	R
CA	Request To Send	RS	Request To Send	105	R
CB	Clear To Send	CS	Clear To Send	106	R
CF	Received Line Signal Detector	RR	Receiver Ready	109	D
CG	Signal Quality Detector	SQ	Signal Quality	110	D
CH	Data Signal Rate Selector (DTE Source)	SR	Signaling Rate Selector	111	D
CI	Data Signal Rate Selector (DCE Source)	SI	Signaling Rate Indicator	112	D
LL	Local Loopback	LL	Local Loopback	141	L
RL	Remote Loopback	RL	Remote Loopback	140	R
TM	Test Mode	TM	Test Mode	142	T

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: either the software reacts to a received signal when it changes, or the software can assert a transmitted signal when necessary (such as LL which can be used by operations personnel for testing connections). Unsupported circuits are either not read by the software or a value is written to the circuit by the software, and that value does not change during operation. Table 7-2 provides a list of circuits and their use.

(3) Interchange Circuit Definitions.

(a) Signal Ground. See EIA Standard 232-D.

(b) DCE Ready. This circuit is not monitored by the PSN software.

(c) DTE Ready. This circuit is asserted OFF by PSN software when the link is initialized. Available for Monitoring Center control.

(d) Transmitted Data. See EIA Standard 232-D.

(e) Received Data. See EIA Standard 232-D.

(f) Transmitter Signal Element Timing (DCE Source). See EIA Standard 232-D. This circuit provides the clock for Transmitted Data when the DCE sources timing.

(g) Receiver Signal Element Timing (DCE Source). See EIA Standard 232-D. This circuit provides clock for Received Data when the DCE sources timing.

(h) Request to Send. This circuit is asserted OFFby PSN software when the link is initialized. Available for Monitoring Center control.

(i) Clear to Send. This circuit must be asserted ON by the DCE, but it is not monitored by the PSN software.

(j) Received Line Signal Detector. This circuit must be asserted ON by the DCE, but it is not monitored by the PSN software.

3. Mechanical Characteristics. The MMR EIA-232-D connectors on the C/30E meets the specifications provided in this section.

a. Interface Connectors. The MMR C/30E fantail EIA-232-D connector is a DB-25P type (male) connectors. Intermating dimensions are in accordance with EIA-232-D, section 3.2.1.

b. Connector Contact Assignments. DDN standard node EIA-232-D connector contact assignments are in accordance with EIA-232-D, section 3.3.1. Table 7-3 provides DDN EIA-232-D connector pin assignments. Signal use is specified in section 2.d.3. of this Standard.

TABLE 7-2. EIA-232-D INTERCHANGE TRUNK CIRCUIT USE

232 ID	EIA-232-D Name	Source	Electrical State	Required State of Control/Status Signals	Comments
AB	Signal Ground	DTE/DCE	Ground	N/A*	
BA	Transmitted Data	DTE	Active	N/A	
BB	Received Data	DCE	Active	N/A	
CA	Request to Send	DTE	Active	OFF	
CB	Clear to Send	DCE	Active	Don't Care	
CC	DCE Ready	DCE	Active	Don't Care	
CD	DTE Ready	DTE	Active	OFF	
CF	Received Line Signal	DCE	Active	Don't Care	
DB	Transmitter Signal	DCE	Active	N/A	
DD	Receive Signal Element Timing	DCE	Active	N/A	

* N/A = Not Applicable

TABLE 7-3. EIA-232-D CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
1	--	--	Shield
2	BA	103	Transmitted Data
3	BB	104	Received Data
4	CA	105	Request To Send
5	CB	106	Clear To Send
6	CC	107	DCE Ready
7	AB	102	Signal Ground (Common Return)
8	CF	109	Received Line Signal Detector
9	--	---	+ DC Test Voltage (+8VDC)
10	--	---	- DC Test Voltage (-8VDC)
11	DB	114	Transmitted Signal Element Timing (DCE Source)
12	DD	115	Receiver Signal Element Timing (DCE Source)
13	CD	108/2	DTE Ready

* The circuit name "DC" is from and earlier version of EIA-232.

4. Interconnecting Cables.

a. For interconnecting cable specifications, see chapter 1 and section 4, of this guide.

b. Figure 7-1 is a cabling diagram of a C/30E PSN connected to a nearby EIA-232 PSN, and figure 7-2 is an example of an interconnecting cable (BBNCC P/N# 2405535G01).

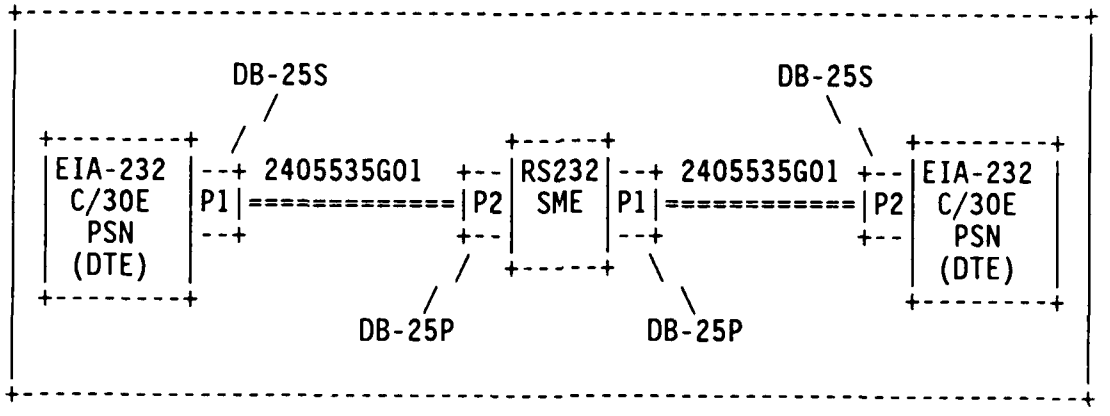


FIGURE 7-1. C/30E PSN AND NEARBY EIA-232-D PSN CABLING DIAGRAM

CHAPTER 8. V.35 REMOTE TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the obsolete DDN V.35 connection between two remote PSNs. DDN standard does not support neighbor or nearby V.35 PSN-PSN connections. Like the EIA-232 interface, the V.35 interface is used only where an existing non-DDN-standard PSN provides such an interface, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN-standard (MIL-STD-188-114 balanced serial PSN interfaces). All control signals have electrical characteristics of EIA-232-D, and EIA-232-D signal names are used in the rest of this chapter. The data and timing signals conform to Recommendation V.35. DDN supports Extended Modem Looping (XMOD) through the V.35 interface.

2. Electrical Characteristics.

a. Voltage Levels. The electrical measurements of the C/30E V.35 interface circuits are in accordance with CCITT Recommendation V.35.

b. Clocking. The MMV interface hardware contains the connectors that terminate the cables from all I/O interfaces. The MMV fantail contains one V.35 connector configured as a DTE. This interface has no clock-sourcing capability. The hardware can support external clock rates between 300 b/s and 100 kb/s.

(1) Signaling Sense. Signaling sense is in accordance with CCITT Recommendation V.35. A binary "0" (space) is transmitted when terminal "A" is positive (+.55v ±20%) to terminal "B" (-.55V ±20%). A binary 1 is transmitted when terminal "A" is negative (-.55v ±20%) to terminal "B" (+.55v ±20%). The drivers produce a nominal 1.1 volts peak-to-peak signal balanced with respect to ground.

c. Bit Rate/Cable Length.

(1) Maximum Cable Length. The recommended maximum cable length between a V.35 DCE and DTE is 30 feet when overall shielded, low capacitance, twisted pair cable is used. Cable lengths of up to 2000 feet are also possible with the proper cables, see LOR-0023-003 for more details.

d. Interchange Circuits.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in Table 8-1.

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are

under program control: either the software reacts to the circuit signal when it changes, or the software can assert a circuit when necessary (such as LL which can be used by operations personnel for testing connections). Unsupported circuits either are not read by the software or a value is written to the circuit by the software, and that value does not change during operation. Table 8-1 describes circuit use.

(3) Interchange Circuit Definitions. EIA-232-D signal names are used throughout this chapter.

(a) Signal Ground. See EIA-232-D.

(b) DCE Ready. This circuit must be asserted ON by the DCE, but it is not monitored by the PSN software.

(c) Transmitted Data. See EIA-232-D.

(d) Received Data. See EIA-232-D.

(e) Transmitter Signal Element Timing (DTE Source). See EIA-232-D. Also see subsection 2.b of this guide. This circuit provides the clock for Transmitted Data when the PSN sources timing. The frequency of this circuit is equal to that of Transmitter Signal Element Timing.

(f) Transmitter Signal Element Timing (DCE Source). See EIA-232-D. This circuit optionally provides the clock for Transmitted Data when the DCE sources timing.

(g) Receive Signal Element Timing (DCE). This circuit optimally provides the clock for received data when the DCE sources timing.

(h) Request to Send. This circuit is asserted OFF by the PSN software. Available for Monitoring Center control.

(i) Clear to Send. This circuit must be asserted ON by the DCE, but it is not monitored by PSN software.

(j) Received Line Signal Detector. This circuit must be asserted ON by the DCE, but it is not monitored by PSN software.

(k) Data Terminal Ready. This circuit is asserted OFF by the PSN software. Available for Monitoring Center control.

(l) Local Test Loopback. This circuit is asserted OFF by the PSN software. Available for Monitoring Center control.

TABLE 8-1. V.35 TRUNK INTERCHANGE CIRCUIT USE

CCITT ID	Name	Source	Electrical State	Required State of Control/Status Signals	Comments
101	Protective Ground	DTE/DCE	Ground	N/A	
102	Signal Ground	DCE/DTE	Ground	N/A	
103	Transmitted Data	DTE	Active	N/A	
104	Received Data	DCE	Active	N/A	
105	Request to Send	DTE	Active	OFF	
106	Clear to Send	DCE	Active	ON	
107	DCE Ready	DCE	Active	Don't Care	
108/2	DTE Ready	DTE	Active	OFF	
109	Received Line	DCE	Active	ON	
113	Transmitter Signal Element Timing	DTE	Active	N/A	
114	Transmitter Signal Element Timing	DCE	Active	N/A	
115	Receiver Signal Element Timing	DCE	Active	N/A	
141	Local Test Loopback	DCE	Active	OFF	

NOTES: N/A = Not Applicable

3. Mechanical Characteristics. All V.35 connectors offered for the C/30E meet the specifications provided in this section. Cables for this interface, supplied by DDN, are equipped with an EIA-449 connector on one end to mate with the EIA-449 connector on the C/30E fantail; the other end provides a MIL-C-28748 34-pin connector to mate with the V.35 DCE.

a. Interface Connectors. The V.35 connectors on the C/30E fantail is a DC-37P type (male) connector. It is wired as described in Table 8-2.

(1) Intermating dimensions are in accordance with EIA-449-D.

(2) The means for C/30E DTE connectors to latch and unlatch from the latching blocks on the DCE connector are within the dimensions specified in EIA-449, section 3.3.1. DDN uses the English 4-40 thread latching block.

b. Connector Contact Assignments. DDN standard node V.35 connector contact assignments are in accordance with CCITT Recommendation V.35 and ISO 2593. Table 8-2 provides DDN V.35 connector pin assignments. The signals are used as specified in section 2.d.3.

4. Interconnecting Cables.

(a) For interconnecting cable specifications, see chapter 1, section 4, of this guide.

(b) Figure 8-1 is a cabling diagram of a V.35 PSN and remote V.35 PSN, and figure 8-2 provides an example of an interconnecting cable (BBNCC P/N# 2405510G01).

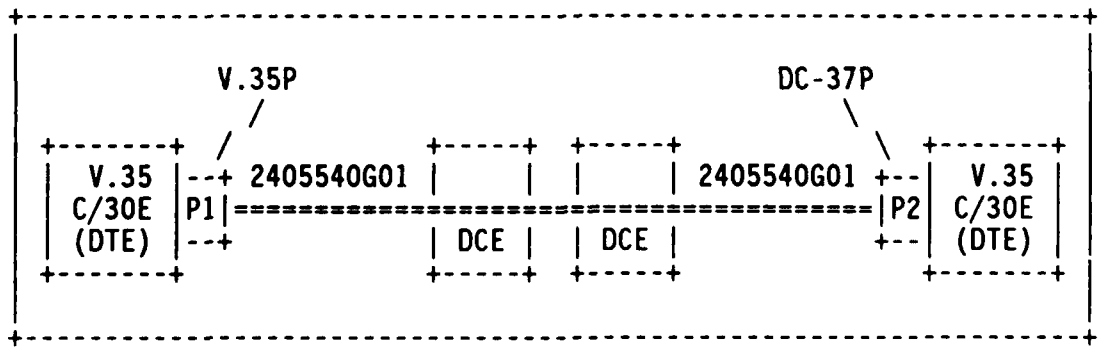


FIGURE 8-1. C/30E PSN AND REMOTE V.35 PSN CABLING DIAGRAM

TABLE 8-2. V.35 34-PIN AND 37-PIN CONNECTOR PINOUT

34-pin #	37-pin* #	CCITT ID	Signal Name	449 Name
A	1	101	Shield	FG
P	4	103	Transmitted Data	SD+
S	22	103	Transmitted Data	SD-**
Y	5	114	Transmitter Signal Element Timing (DCE Source)	ST+
a/AA	23	114	Transmitter Signal Element Timing (DCE Source)	ST-
R	6	104	Received Data	RD+
T	24	104	Received Data	RD-
V	8	115	Receiver Signal Element Timing (DCE Source)	RT+
X	26	115	Receiver Signal Element Timing (DCE Source)	RT-
H	30	108/2	DTE Ready	TR
B	12	102	Signal Ground	SG
C	7	105	Request to Send	RS
B***	25	102	Signal Ground	SG
K	10	141	Local Test Loopback	LL(LT)
B	28	102	Signal Ground	SG
U	17	113	Transmitter Signal Elem Timing (DTE Source)	SG-
W	35	113	Transmitter Signal Elem Timing (DTE Source)	SG-
E	11	107	DCE Ready	RR
B	29	102	Signal Ground	SG
D	9	106	Clear to Send	CS
B****	27	102	Signal Ground	SG
F	13	109	Received Ready	RR
B	31	102	Signal Ground	SG
B	19	102	Signal Ground	SG
B	37	102	Signal Ground	SG

* This information represents a straight cable to a V.35 DCE.
** The + and - symbols, used in EIA-449, correspond to A and B, respectively, in V.35 terminology.
*** Internally reflected clocks are supplied on pins TT.
**** V.35 in 34 pin connector is labeled as pin B Signal Ground.

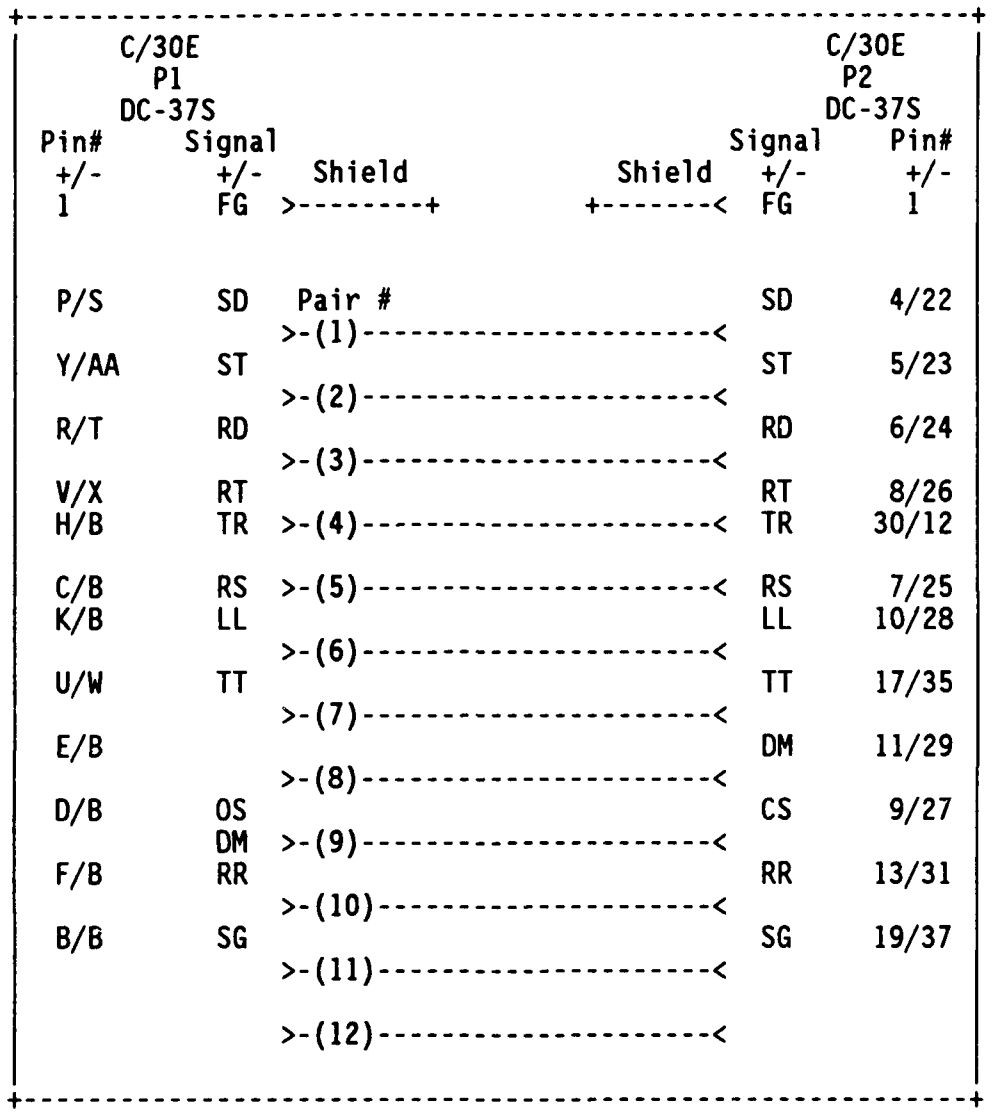


FIGURE 8-2. CABLE EXAMPLE: C/30E PSN TO REMOTE V.35 PSN

CHAPTER 9. BELL 303 NEIGHBOR OR NEARBY TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the BELL 303 DTE interface that connects the C/30E PSN with a modem. This interface is in conformance with the BELL 303 standard, cited in chapter of this guide. The BELL 303 interface is used only where an existing non-DDN-standard PSN provides such an interface, and it is not feasible to install a MIL-STD-188-114 balanced interface prior to upgrading the entire node to DDN-standard (MIL-STD-188-114 balanced serial PSN interfaces). DDN supports Extended Modem Looping (XMOD) through the BELL 303 interface. For ease of reference, table 9-1 equates the EIA-449, BELL 303, and CCITT interface signal names. In the remainder of the BELL 303 discussion, the EIA-449 signal name will be used.

2. Electrical Characteristics.

a. Voltage Levels and Signaling Sense. The electrical measurements of the C/30E interface circuits are in accordance with Bell 303. The cable drivers operate into, and the cable terminators operate from coaxial cables, with 75 ohms to 120 ohms characteristic impedance. The high speed interface is provided on a current switching basis. A binary "1", Control "OFF" or "marking" signal is represented by a current less than 5 ma into 100 ohms. A binary "0", Control "ON" or "spacing" signal is represented by a current greater than 23 ma into 100 ohms. All interchange circuits are fail-safe in that an open circuit is considered a control OFF or Mark Hold condition.

The above-mentioned currents are supplied at the output of the cable drivers. The open circuit voltage of the terminator will range between -1.3 and -0.8 volts. The negative voltage is added by a bias in the terminator. With greater than 23 ma into 100 ohms supplied to a cable terminator, the terminator input voltage is more positive than +1.0 volts. An open circuit must be recognized by a terminator as OFF, as mentioned above.

TABLE 9-1. SIGNAL NAME EQUIVALENCY TABLE

EIA-449 ID	EIA-449 Name	BELL 303 ID	BELL 303 Name	CCITT ID	CCITT Name
SG	Signal Ground	--	Ground in Sleeves	102	Signal Ground
SC	Send Common	--		102a	DTE Common
RC	Receive Common	--		102b	DCE Common
SD	Send Data	E	Send Data	103	Transmitted Data
RD	Receive Data	K	Received Data	104	Received Data
RS	Request To Send			105	Request To Send
CS	Clear To Send			106	Ready For Sendin
DM	Data Mode			107	Data Set Ready
TR	Terminal Ready				
				108/2	Data Terminal Re
RR	Receiver Ready			109	Data Channel Rec Signal Detector
IS	Terminal In Service	--		---	
SR	Signaling Rate Selector			111	Data Signaling R Selector (DTE S
SI	Signaling Rate Indicator			112	Data Signaling R Selector (DCE S
NS	New Signal	--		---	
TT	Terminal Timing			113	Transmitter Sign
ST	Send Timing	J	Serial Clock Transmit	114	Transmitter Sign Timing (DCE Sou
RT	Receive Timing	L	Serial Clock Receive (DCE Source)	115	Receiver Signal Timing (DCE Sou
SS	Select Standby	--		116	Select Standby
SF	Select Frequency	--		126	Select Transmit
LL	Local Loopback	G	Local Test	141	Local Loopback
RL	Remote Loopback			140	Remote Loopback

b. Clocking. Two fantails, MMI and MML, provide the connectors that terminate cables from all I/O interfaces. The MMI fantail connector is configured as a DTE. When the MMI fantail is used, the DCE must provide clock because the MMI fantail does not support clock-sourcing capability. The MML, a clock-sourcing enhanced fantail, is configured as a DCE and provides clock.

(1) MML Clock Rates. MML and MMI interface hardware support any external clock between 1.2 kb/s and 112 kb/s. However, DDN policy states that the minimum PSN bit rate be 9.6 kb/s. When MML clock-sourcing capability is used, the MML on-board clock generator provides the following frequencies: 230.4 kb, 50 kb, 19.2 kb. The 230.4 kb rate is not supported by operational software.

(2) Maximum Cable Length. The maximum length of the cable is 50 feet. The MMI-configured PSN connector has a DC-37P type (male) as the DTE and the MML-configured PSN connector has a DC-37S (female) as the DCE. Cable lengths greater than 200 feet may be possible. The BELL 303 specification, section 7, should be consulted.

d. Interchange Circuits. The BELL 303 interface is provided by the MMI motherboard upon which is attached an MMI/MML daughterboard.

(1) Electrical Use of Interchange Circuits. The DDN electrical use of interchange circuits is either static or active. Static circuits are tied by the hardware so that the signal state remains constant on the line, either ON or OFF. Active circuits change their state under program control. DDN use of the interchange circuits is shown in table 9-2.

(2) Software Use of Interchange Circuits. Interchange circuit signals are used by the software in different ways. Active circuits are under program control: the software can react to a received signal when it changes, and the software can assert a transmitted signal when necessary (such as LL, which can be used by operations personnel for testing connections). Unsupported circuits either are not read by the software or a value is written to the circuit by the software. That value does not change during operation. Table 9-2 provides a list of circuits and their use.

(3) Interchange Circuit Definitions. For additional information about these interchange circuits, see EIA Standard 449. The following descriptions assume use of full period/full duplex circuits, with flow control handled at higher levels.

(a) Signal Ground. See EIA Standard 449.

(b) Send Data. See EIA Standard 449.

(c) Receive Data. See EIA Standard 449.

(d) Send Timing. See EIA Standard 449.

(e) Receive Timing. See EIA Standard 449.

(f) Local Loopback. LL is asserted OFF by PSN software when the link is initialized. LL can be controlled by the Monitoring Center.

TABLE 9-2. BELL 303 TRUNK INTERCHANGE CIRCUIT USE

449 ID	EIA-449 Name	Source	Electrical Circuit	Required State of Control/Status Signals	Comments
SG	Signal Ground	DTE/DCE	Ground in Sleeve	N/A	Ground
SD	Send Data	DTE	Active	N/A	Data Circuit
RD	Receive Data	DCE	Active	N/A	Data Circuit
ST	Send Timing	DCE	Active	N/A	Timing circuit for Data when DCE prov
RT	Receive Timing	DCE	Active	N/A	Timing circuit for Data when DCE prov
LL	Local Loopback	DTE	Active	OFF	Initialized to OFF Available for Moni Control through XM

NOTE: N/A = Not Applicable

3. Mechanical Characteristics. All BELL 303 connectors offered for the C/30E meet the following specifications.

a. Interface Connectors. The C/30E MMI/MML BELL 303 connector DC-37P type (male) connectors.

(1) Intermating dimensions are in accordance with EIA Standard 449, section 3.3.1.

(2) The means for C/30E DTE connectors to latch and unlatch from the latching blocks on the DCE connector are within the dimensions specified in EIA Standard 449, section 3.3.2. DDN uses the English 4-40 thread latching block.

b. Connector Contact Assignments. All C/30E BELL 303 contact assignments, as shown in table 9-3, provide the DDN standard node connector pinout. The signals are used asspecified in EIA Standard 449 section 2.d.3.

TABLE 9-3. DDN STANDARD NODE EIA-449 (DTE) CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
8	SD	103	Send Data
27	SG	102	Signal Ground
12	ST	114	Send Timing
31	SG	102	Signal Ground
10	RD	104	Receive Data
29	SG	102	Signal Ground
6	RT	115	Receive Timing
25	SG	102	Signal Ground
11	LL	141	Local Loopback
30	SG	102	Signal Ground

4. Interconnecting Cables.

a. Interconnecting cables must be low capacitance, multiple twisted pair that result in a transmission line with a nominal characteristic impedance on the order of 100 ohms to frequencies greater than 100 kHz, and a dc series loop resistance not exceeding 240 ohms. The overall braid shield must have at least 85% coverage.

(1) Conductor Size. Interconnecting cables or wires should be composed of wires of a 24 AWG or larger conductor for solid or stranded copper wires, or for non-copper conductors a sufficient size to yield a dc wire resistance not to exceed 30 ohms/1000 feet per conductor.

(2) Mutual Pair Capacitance. The capacitance between one wire in the pair to the other wire in the pair should not exceed 20 picofarads/foot, and the value should be reasonably uniform over the length of the wire or cable.

(3) Stray Capacitance. The capacitance between one wire in the cable to all others in the cable sheath, with all others connected to ground, should not exceed 40 picofarads/foot,and should be reasonably uniform for a given conductor over the length of the wire or cable.

(4) Pair-to-Pair Balanced Crosstalk. The crosstalk from on pair of wires to any other pair in the same cable sheath should have a minimum value of 40 dB attenuation measured at 150 kHz.

b. Figure 9-1 is a cabling diagram of a C/30E PSN connected to a nearby BELL 303 PSN, and figure 9-2 is an example of a cable used to interconnect them.

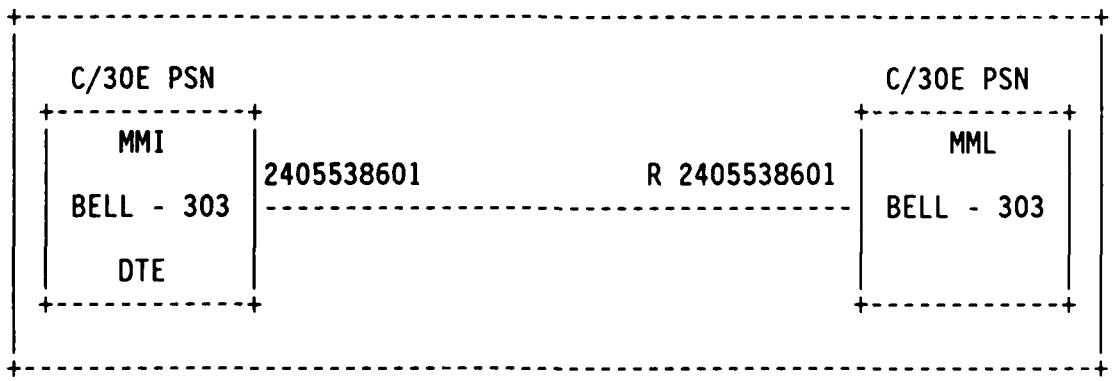


FIGURE 9-1. BELL 303 MMI TO BELL 303 MML CABLING EXAMPLE

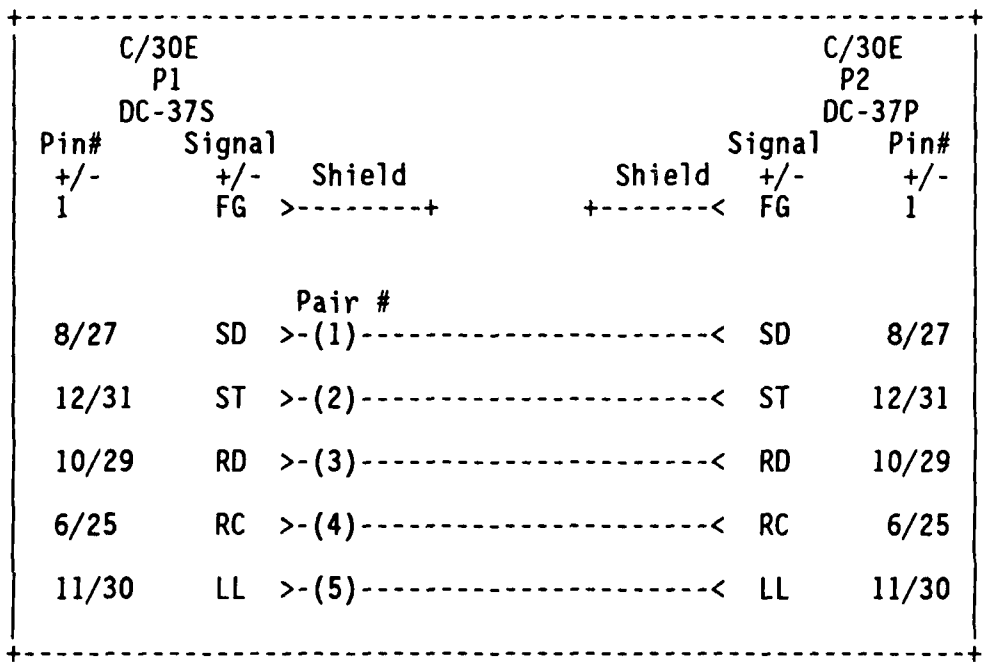


FIGURE 9-2. BELL 303 TRUNK INTERFACE CABLING EXAMPLE

CHAPTER 10. BELL 303 REMOTE TRUNK INTERFACE

1. Overview. This chapter describes the electrical and mechanical characteristics of the BELL 303 balanced remote trunk interface. This chapter documents the interface between the remote modem and the PSN (demarcation point A in figure 10-1)with no intervening cryptographic devices (KG-84As). The DDN standard is a MIL-STD-188-114 balanced interface, and the BELL 303 is used only when it is not feasible to install the standard. DDN supports Extended Modem Looping (XMOD) through the BELL 303 interface.

2. Electrical Characteristics.

a. Voltage Levels and Signaling Sense. The modems used will conform to BELL 303.

b. Clocking.

(1) Modem Clocking. The modem supplies timing on the Send Timing and Receive Timing circuits. Terminal Timing isnot supported for remote PSN interfaces. While the DDN hardware will support between 1.2 kb/s and 64 kb/s, DDN policy is that the minimum PSN access rate be 9.6 kb/s.

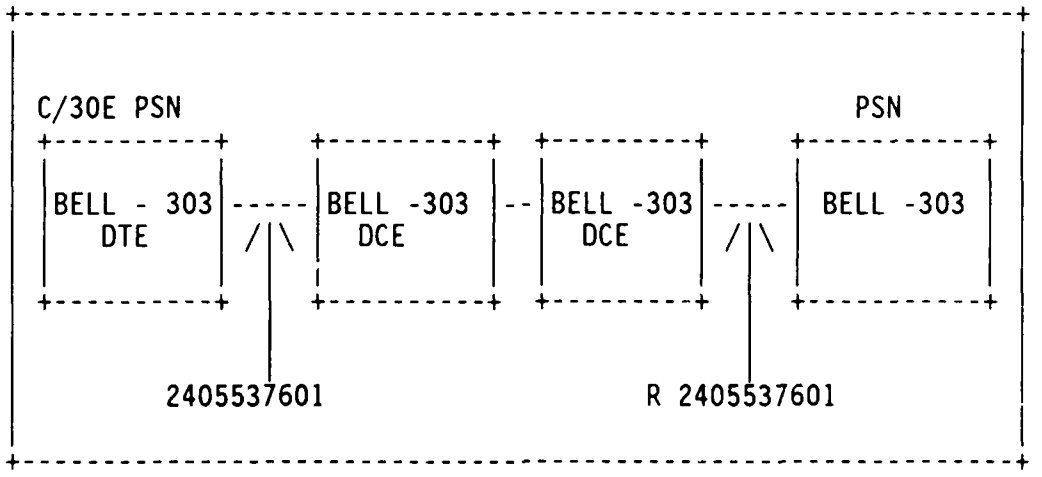


FIGURE 10-1. DEMARCATION POINT "A" BETWEEN THE C/30E AND REMOTE C/30E

c. Bit Rate and Cable Length.

(1) Maximum Cable Length. The maximum cable length between the remote modem and the PSN is 50 feet; however, in some special applications cable lengths more than 200 feet are possible. Refer to the BELL 303 specification section 7.0 for details.

d. Interchange Circuits.

(1) C/30E Local Modem Interface.

(a) Signal flow between the C/30E and the local modem is shown in figure 6-3. This interface and associated hardware are provided by DDN. This DCE interface uses BELL 303 pin assignments.

(b) As shown in figure 10-2, the supported signals are Send Data (SD), Serial Clock Transmit (ST), Receive Data (RD), and Serial Clock Receive (SR) and Local Test (LL).

3. Mechanical Characteristics.

a. Interface Connectors. The PSN end of the cable has a connector of the DC-37S type (female) and the DCE end of the cable connector has a Burndy MD12MXP-17TC plug with a Burndy M2H50RC-1P2 protective shield.

b. Connector Contact Assignments. Table 10-1 provides the standard DTE pinouts. Table 10-2 provides the standard DCE pinouts, and section 2.d.3 of the EIA Standard 449 provides circuit descriptions.

TABLE 10-1. DTE INTERFACE CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
8	SD	103	Send Data
27	SG	102	Signal Ground
12	ST	114	Send Timing
31	SG	102	Signal Ground
10	RD	104	Receive Data
29	SG	102	Signal Ground
6	RT	115	Receive Timing
25	SG	102	Signal Ground
11	LL	141	Local Loopback
30	SG	102	Signal Ground

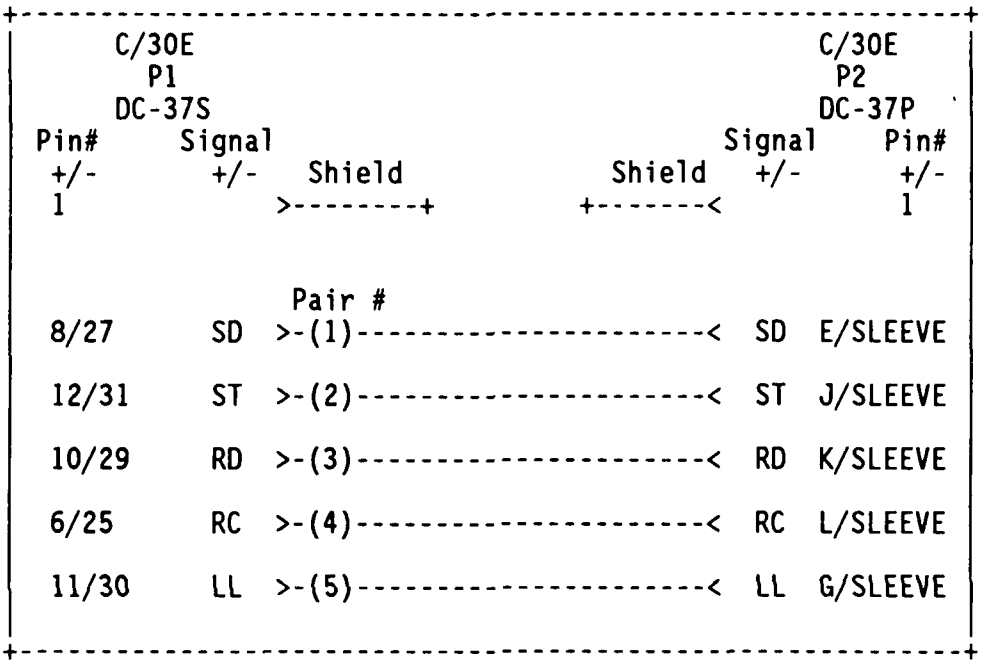


FIGURE 10-2. BELL 303 REMOTE TRUNK INTERCHANGE CIRCUIT USE

TABLE 10-2. DCE BELL 303 INTERFACE CONECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
E	SD	103	Send Data
SLEEVE	SG	102	Signal Ground
J	ST	114	Send Timing
SLEEVE	SG	102	Signal Ground
K	RD	104	Receive Data
SLEEVE	SG	102	Signal Ground
L	RT	115	Receive Timing
SLEEVE	SG	102	Signal Ground
Optional			
G	LL	141	Local Loopback
SLEEVE	SG	102	"D" Loop (Reserved)

TABLE 10-3 KGAB - REMOTE MODEM CONNECTOR PINOUT

Pin	EIA ID	CCITT ID	Name
Mandatory			
1	FG		Frame Ground
2	SD +	103	Send Data
3	SD -	103	Send Data
4	ST +	114	Send Timing
5	ST -	114	Send Timing
6	RD +	104	Receive Data
7	RD -	104	Receive Data
8	RT +	115	Receive Timing
9	RT -	115	Receive Timing
10	TR +	108.2	Terminal Ready
11	TR -	108.2	Terminal Ready
14	SG	102	Signal Ground
15	SG	102	Signal Ground
24	TT +	113	Terminal Timing
25	TT -	113	Terminal Timing
Optional			
12	CS +	106	Clear to Send
13	CS -	106	Clear to Send
16	CL +	---	"C" Loop (KG-84A Loop)
17	CL -	---	"C" Loop (KG-84A Loop)
18	RL +	140	Remote Loopback
19	RL -	140	Remote Loopback
20	DL +	---	"D" Loop (Reserved)
21	DL -	---	"D" Loop (Reserved)
22	LL +	141	Local Loopback
23	LL -	141	Local Loopback

4. Interconnecting Cables. Figure 10-1 provides a cabling diagram of a configuration with a C/30E and a BELL 303 modem. Table 10-3 describes the cable used for interconnecting these devices.

TABLE 10-4. REMOTE INTERFACE CABLES

Connection	BBNCC P/N#	Description
PSN IMP/MII to BELL 303	2405537G01	5-pr, PSN/MII BELL 303 to BELL 303 Modem